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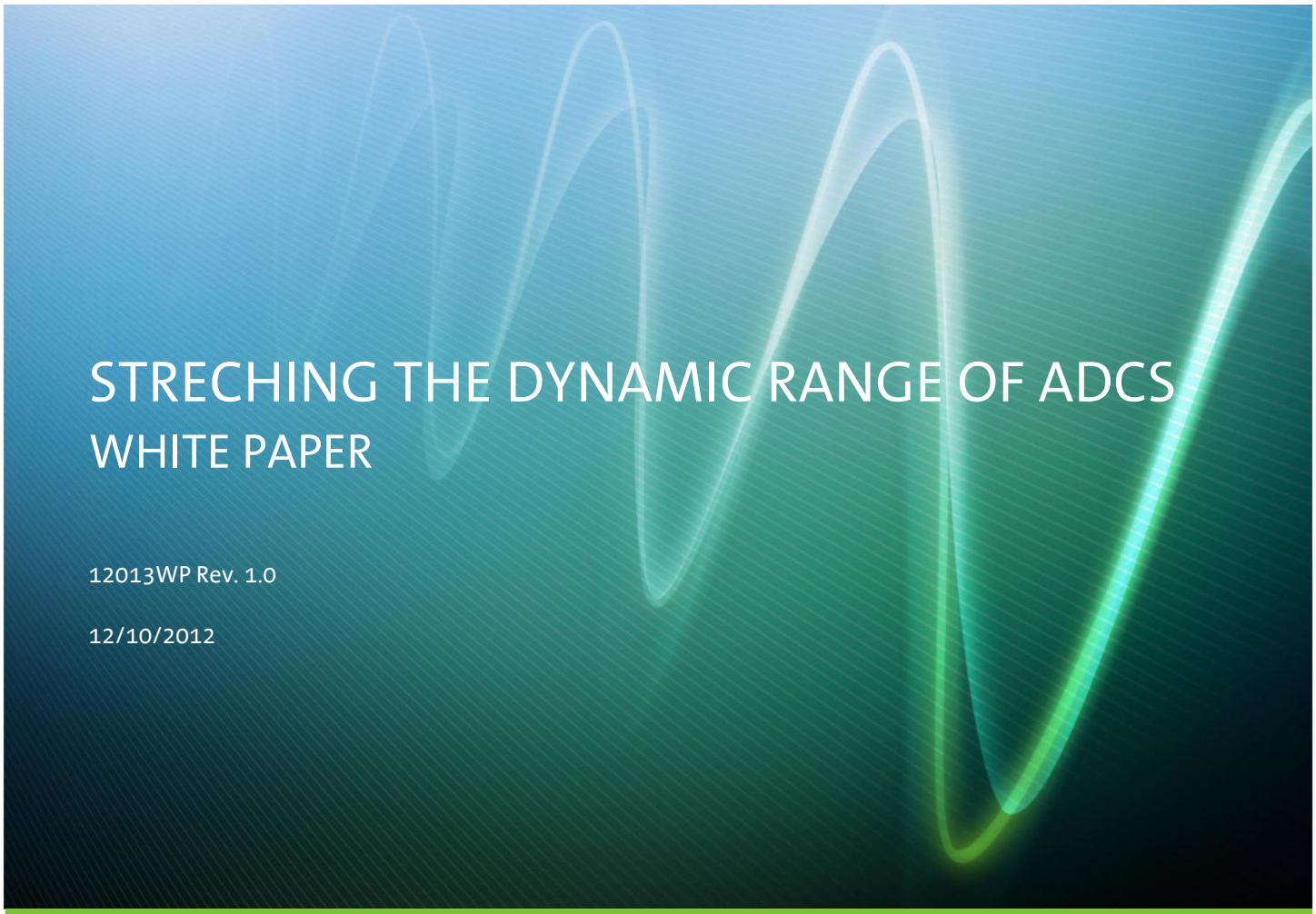
SIGNAL PROCESSING **IQ** : **FPGA** EXPERTISE



STRECHING THE DYNAMIC RANGE OF ADCS
WHITE PAPER

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Whether your application is focussed on EW, wireless communications or instrumentation, the performance bottleneck is often the dynamic range of the analogue to digital converter (ADC). Dynamic range is often a key parameter within signal processing systems and a shortfall can limit the quality and range of signals that can be received. The technical progress made on improving this gateway between the analogue and digital world has not kept pace with Moore's law[1] because the challenges are more fundamental than simply reducing transistor sizes. Methods to increase ADC dynamic range are therefore always of interest although each solution often suits particular usage scenarios.

As an example of pushing ADC dynamic range beyond what is currently available, the engineers at RFEL were confronted with an application where the customer required an analogue to digital conversion with a 74dB dynamic range at 800MSPS. Most available ADCs at this rate were typically 52dB, i.e. 8.3 effective number of bits[2] (ENOB). This was a significant 22dB shortfall which had to be resolved for the project to be feasible.

Various techniques for extending dynamic range were considered taking into account their advantages and disadvantages:

1. Increase the sample rate. The quantisation noise floor of an ADC can be reduced by sampling at a higher rate and subsequently decimating the output. This has the effect of averaging out incoherent noise sources and in theory the dynamic range can be increased by 3dB for each doubling of sample rate. However at higher sample frequencies the gains are modest because the ENOB performance of high rate ADCs also degrade. The ADC cost should also be considered as this usually increases with sample rate.
2. Interleaved ADCs. A more common solution is to use multiple lower rate ADCs, which inherently have a better ENOB, to consecutively sample the input signal in an interleaved manner. The dynamic range gains are very much dependent upon the ENOB improvement of the lower rate converters which tends to be more significant when targeting high sample rates. To retain any performance gains, careful consideration must be given to amplitude and phase matching between ADCs. This can involve gain matching, PLL selection and attention to PCB layout.
3. Non-linear gain stage. If the input signal is passed through a device with a non-linear gain, then the target dynamic range of the input signal can be mapped onto the available input range of the ADC. This effectively produces an ADC quantisation step size which increases with the amplitude of the input signal. A disadvantage of this technique is that the signal must be restored by subsequent signal processing which often requires signal training to guarantee accuracy. Also quantisation noise is dominated by the largest part of the signal.
4. Stacked ADCs. To make a significant improvement in dynamic range, a stacked ADC architecture can be used. In this approach, the signal is split into multiple paths, each with a different gain before input to the ADC. If for example three ADCs are used, they would capture large, medium and small signals respectively and the final output would be selected from the most appropriate ADC. This principle has an obvious problem because although one signal can be tracked over a large dynamic range, the instantaneous dynamic range (i.e. the capability to receive large and small signals at the same time) is actually degraded. Another potential issue is that each path must be carefully matched to align phase, amplitude and frequency responses.

For the project, the large 22dB increase in dynamic range could not be realistically achieved using (1) or

[1] Moore's law is infamous for its prediction of the rate at which silicon technology will evolve
[2] The calculation for ENOB is : (dynamic range – 1.76)/6.02

(2). Technique (3) was feasible; however it was rejected due to the large quantisation steps for large input signals and the overhead of signal training. Further analysis of the system requirements revealed that the customers monitoring application did not require a high instantaneous dynamic range, therefore the feasibility of solution (4) was investigated further.

To achieve 74dB of dynamic range requires roughly 12 (74/6) bits, however we also need to add on the minimum signal to noise ratio (SNR) that our system requires which in this case is 4bits. Our total signal range is therefore roughly 16 (12+4) bits. We previously mentioned that phase and amplitude matching was important, therefore we would like to have identical ADCs in a dual, triple or quad packaged IC. The best option considering device cost and performance was an e2v EV8AQ160 - 8bit quad packaged device. To meet the dynamic range and SNR requirements, three of the four packaged ADCs were used to cover the full 16 bit range. The ADCs were allocated such that the most sensitive 'ADC_Low' detects bits 1:8, 'ADC_Mid' detects bits 4:12 and 'ADC_High' detect bits 8:16 (see Figure 1). This covers the full 16bit range fulfilling the dynamic range requirement and provides a four bit overlap to satisfy the SNR requirement.

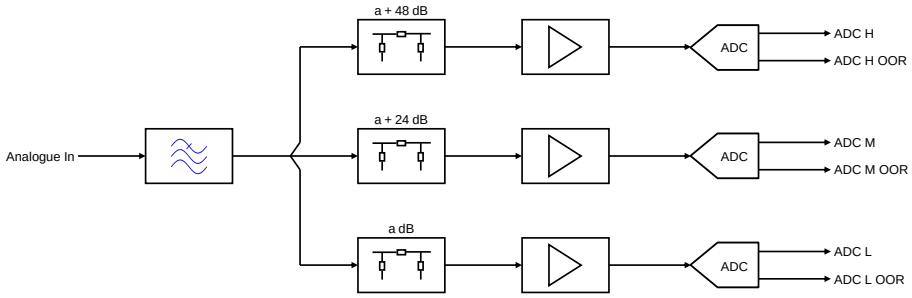

Figure 1: Stacked ADC configuration

The design and layout of the analogue input network is another potential minefield especially because the input signal is split into three different gain paths (see Figure 1). To maintain a consistent amplitude, phase and frequency response each path contains an identical active gain stage which is preceded by a passive attenuator of 0dB, 24dB and 48dB for the high (bits 1:8), medium (bits 4:12) and low (bits 8:16) gain paths respectively. To reduce noise, linear power regulators were used and the high gain signal path was positioned away from other potential sources of noise.

The analogue and digital components were designed, simulated and then fabricated onto a 14 layer PCB. The high layer count was required to enable multiple BGA devices to be routed within a small area. The performance of the design was tested over the complete signal range under various environmental and EMC conditions to ensure robust operation. Figure 2 below shows the combined 16 bit output for an input signal at full scale (low gain path active) and then again after it has been attenuated by 76dB (high gain path active). The pulse shape can clearly be observed in both figures. The second figure shows that our efforts to mitigate noise have paid off as we are successfully operating close to the quantisation noise floor of the device.

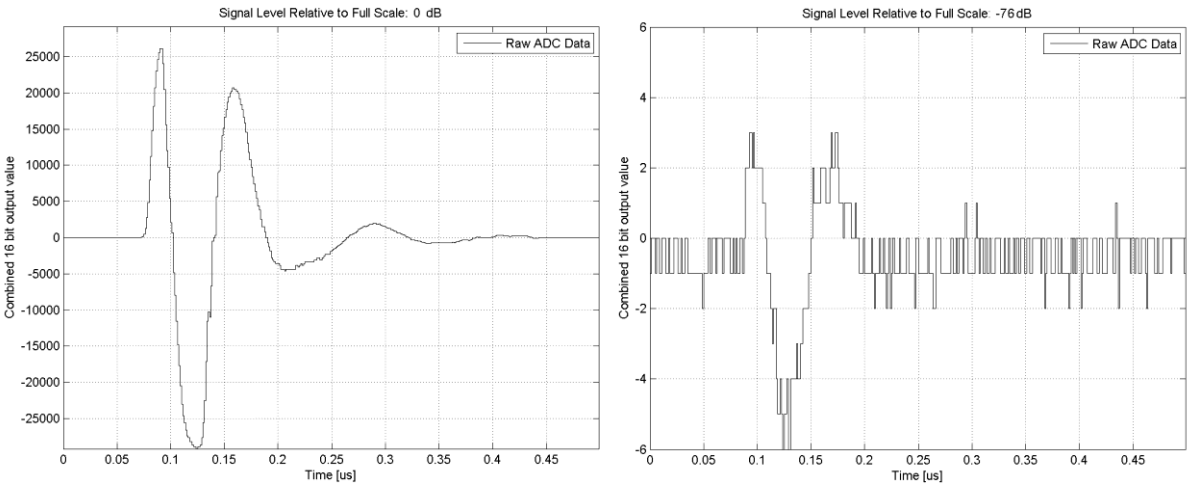

Figure 2: Performance at full scale and full scale -76dB

This article has focused upon extending the dynamic range of the analogue to digital conversion process. In the final product this was the first enabling step before useful information within the input signals could be extracted through digital signal processing. The processing was carried out within multiple high speed FPGAs before results are sent out over a network connection – although this is another story.

About the Author

Robert Fifield, MSc CEng MIET, Senior Digital Systems Design Engineer at RFEL studied at the University of Manchester Institute of Science and Technology (UMIST), where he received a BSc in Electrical and Electronic engineering and an MSc in Instrumentation and Analytical science. He has worked in wireless communications as a Senior Research Scientist at Philips Research Labs (1995-2005), and as a Senior Scientist at NXP Semiconductors UK (2006-2008), before joining RFEL. An active member of ETSI RES10 and BRAN standardisation bodies, he worked on prototype OFDM demonstration systems, and has filed 15 wireless system related patents. As digital processing speeds increased, he was involved with the development of early Software Defined Radio (SDR) architectures, using digital techniques to remove analogue functionality from systems such as GSM, CDMA2000, UMTS, 802.11a/g/n-20/n-40, GPS and Bluetooth.