RF Engines launches ChannelCore64 - achieving 64 reconfigurable DDC Channels in one FPGA

New multi-channel down-converter FPGA core delivers an exciting step improvement in flexible radio channelisation

EMBARGOED UNTIL 24 OCTOBER 2005

GSPx 2005, the Pervasive Signal Processing Event, Santa Clara, CA – October 24, 2005 – RF Engines today introduced the first, fully flexible 64-channel digital down-conversion (DDC) core for use on FPGAs.

ChannelCore64 allows designers to replace up to 16 specialist DDC ASIC devices with a single IP core for FPGA, significantly reducing board area, lowering power consumption, and increasing flexibility. The new approach represents a major cost saving over traditional methods, with savings becoming more significant as the number of channels increases. ChannelCore64 is targeted at applications such as wireless base stations, satellite ground stations, and other multi-channel radio receivers.

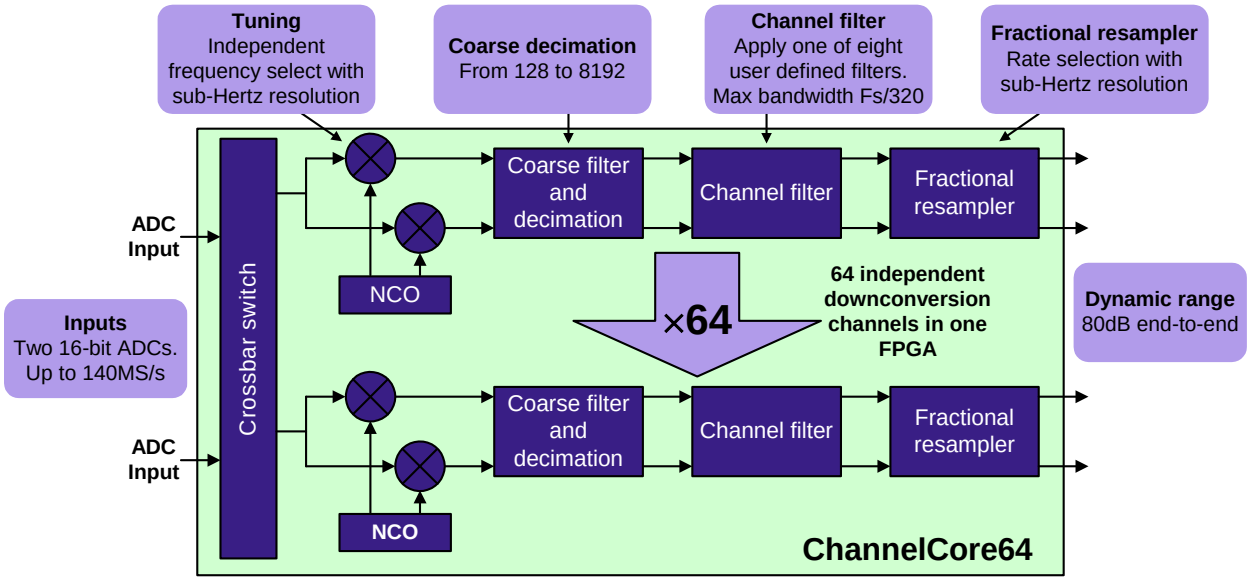
Almost all radio receivers need to extract one or more relatively narrow channels from a much wider input spectrum in a process called down-conversion. The trend towards increased flexibility within this part of the system is enabling interoperability between different radio access technologies, permits dynamic reconfiguration of band-plans, and future-proofs investment in receiver systems. Furthermore, ever increasing user demand for bandwidth coupled with new technologies such as MIMO, means that systems must be capable of supporting an increasing number of channels.

ChannelCore64 utilises a unique approach to down-conversion that achieves massively greater silicon efficiency per channel than other FPGA-based DDC solutions, whilst providing all of the configuration controls that are typically associated with ASIC based DDCs. The core fits comfortably within a Xilinx Virtex II Pro 30 FPGA device. Furthermore, the end-to-end dynamic range offered by the core is significantly better than other available solutions, and a fractional re-sampler is included to allow output sample rates to be precisely configured.

The key features of ChannelCore64 are:

- Support for two 16-bit ADC inputs each with a sample rate up to 140 mega-samples per second.
- 64 independent down-conversion channels, which may be connected to either ADC.
- Independent tuning of channel centre frequencies with a resolution of < 0.01Hz.
- Independent selection channel bandwidths.
- Independent selection output sample rates with a resolution < 0.01Hz.
- Channel reconfiguration when core is running without affecting the operation of other channels.

A bit-true Matlab model is available free of charge which allows designers to accurately simulate ChannelCore64 within their system context. The core is supplied under a simple licensing model, and custom variants, including up-converters, can be produced on request.



RF Engines Limited

RF Engines Limited (RFEL) is a UK based designer, providing high specification signal processing solutions for FPGA, and turnkey receiver solutions for the homeland security, defence, communications and instrumentation markets. Applications include wireless and wireline base stations, satellite communications systems, test and measurement instrumentation, and bespoke wideband receivers.

Further Information

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