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# RF Engines releases a library of high performance FFT Cores for FPGA

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RF Engines Limited (RFEL), the experts in signal processing for FPGA, has today announced a library containing more than sixty Fast Fourier Transform (FFT) cores for use in Xilinx FPGA devices.

The FFT is one of the most popular signal processing algorithms used in modern electronics equipment, and allows a sequence of time-domain samples to be efficiently converted into a frequency representation. RF Engines' library provides FPGA designers with a source of highly optimised high-speed FFT cores that can be quickly and cost-effectively integrated into a design.

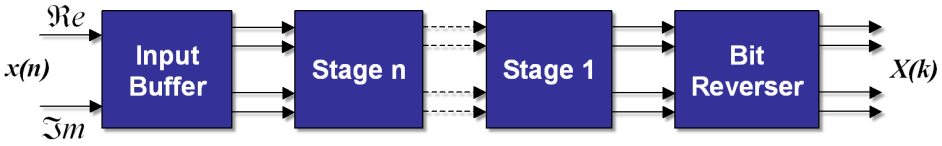
The library is supplied on a single CD, and includes FPGA netlists for a range of FFTs that cover different target devices, transform lengths and sample rates. Cores are provided for Xilinx Spartan III, Virtex II, Virtex II Pro and Virtex 4 FPGA devices, with FFT transform lengths ranging from 32 points, up to 32K points for some device types. Each core can be configured to compute the inverse FFT function, and includes a bit reversal function to allow frequency data to be output in natural order.

Compared to existing FFT generation tools, the FFT library offers options for higher real-time processing speeds, and more silicon efficient options for lower speed requirements. The library also differs from other solutions in the level of support provided to the integrator. Each design includes a bit-true PC simulation, a customised data sheet, and a test bench for the core. Furthermore, the product also includes telephone or email support for integration assistance and advice.

The designs use pipelining techniques that permit the core to run in continuous real-time (streaming I/O) at high sample rates, and two architectures have been used to allow designers to make a trade-off between sample rate and silicon resource usage. The HiSpeed architecture has been used to produce the most silicon efficient cores in the library, and supports complex sample rates up to around 100 MS/s depending on the device type and transform length, whilst cores based on the QuadSpeed architecture support complex sample rates up to 500MS/s in some cases.

RF Engines has used fixed-point arithmetic techniques in order to grow the precision of the data as it progresses through the transform. Thus, for example, a 14-bit integer input grows to around 23-bits by the time it reaches the output of a 32K transform. "Growing" the data in this way ensures that the precision is maintained, whilst use of FPGA resources is kept to a minimum. This approach is markedly different to other available solutions, which use a fixed bit-width from input to output, and often require the designer to sacrifice precision in order to save silicon.

Each core in the library is supplied as an EDIF netlist, and is supplemented with a bit-true Matlab model, a custom data sheet, and a VHDL test bench. The library is supplied with a site-wide licence that permits use for R&D purposes and allows the cores to be shipped in manufactured products.




**RF Engines' FFT Cores use a combination of pipelining techniques and parallelism to achieve optimum performance and minimise FPGA resources**

John Summers, CEO for RF Engines, commented, "Our FFT library provides FPGA designers with a powerful toolkit for quickly adding high speed FFT functionality into designs with the minimum of risk. It includes FFT technology that we have been working for several years to develop and refine, and which has been thoroughly proven in many customer applications. Furthermore, because the library includes such a wide range of cores, and is covered by a simple licensing model, it is likely to be an invaluable investment for future projects."

RFEL also provides a range of signal processing cores that may be used to complement the FFT cores, including programmable window functions, power conversion, accumulation, CORDIC algorithms, and fixed-to-floating-point conversion. The company's Distributed Half Band Filter (DHBF) provides an efficient mechanism for converting a digitised signal from an ADC into a complex representation for input to the FFT transform.

To meet more demanding FFT requirements, the company also provides its HyperSpeed FFT cores, which support sample rates up to 3.2 GS/s, and HyperLength FFT cores, which enables transform sizes up to 256M complex points. For applications that require a non-power-of-two transform length, the company provides its Matrix range of mixed-radix DFT designs.

These FFT cores form only one part of the RFEL product portfolio, which also includes complete system-on-chip designs, as well as COTS-based board solutions for a range of high specification applications

**RF Engines**

RF Engines Limited (RFEL) is a UK based designer, providing high specification signal processing cores, system on chip designs, and FPGA based board solutions for applications in the defence, communications and instrumentation markets. These applications include base stations, wireless and wireline broadband communications systems, satellite communications systems, test and measurement instrumentation, as well as defence systems. More specifically, RFEL is a solutions provider for projects requiring complex front end, real time, wide and narrow band, flexible channelisation. RFEL provides a range of standard cores covering multiple FFT and unique PFT techniques, as well as system design services for specialist applications.

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