



## RF Engines launches dynamically re-configurable radio spectrum channeliser

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RF Engines Limited (RFEL), the UK based signal processing specialist, has just released a radical new patented filter bank design, called **Tuneable Pipelined Frequency Transform™ (TPFT)** to add to its existing range of high performance real-time signal processing architectures.

The **TPFT** allows the user to dynamically select sections of spectrum (channels) of differing bandwidths, from a broad band of spectrum, and to acquire and process these channels in real time. Furthermore, the design disregards the processing of those sections of spectrum that are not of interest, so improving the silicon efficiency even further.

The **TPFT** architecture has been developed by building upon RFEL's own **Pipelined Frequency Transform™** design, and is aimed at those applications that require flexibility in frequency channelisation, but also real-time reconfiguration to different frequency plans.

The **TPFT** is targeted at a range of applications where reconfigurable front ends are required, from wideband multi-standard receivers e.g. satellite earth station receivers, base station receivers, reconfigurable radio systems through to instrumentation. It is aimed at those applications requiring the channelisation of wideband signals (~80MHz) into different size frequency bins arbitrarily distributed across the input spectrum.

The **TPFT** gives the users the freedom to tailor the design to their requirements, and allows them to specify channels by centre frequency and bandwidth, to fully define the filter characteristics, and to then reconfigure in real-time to a different frequency plan or plans, as required. Furthermore, spectral shaping masks can also be directly applied onto the outputs within the architecture itself, so allowing even the final filter shapes to be finely tuned to the needs of the application.

The underlying concept of this architecture is that of successive band splitting in a pipelined manner: at each stage, the input spectrum is split in multiple channels. A first stage splits the input in two frequency bands, a second stage into four, and so on. Tuneability is achieved by controlling the channelisation process from outside the **TPFT** itself, thus allowing reconfiguration on demand. A PC Windows based Graphical User Interface (GUI) controls the architecture (see Figure 1 overleaf), modifying the required parameters as required, although the development of a self-contained SoC architecture is also under consideration.

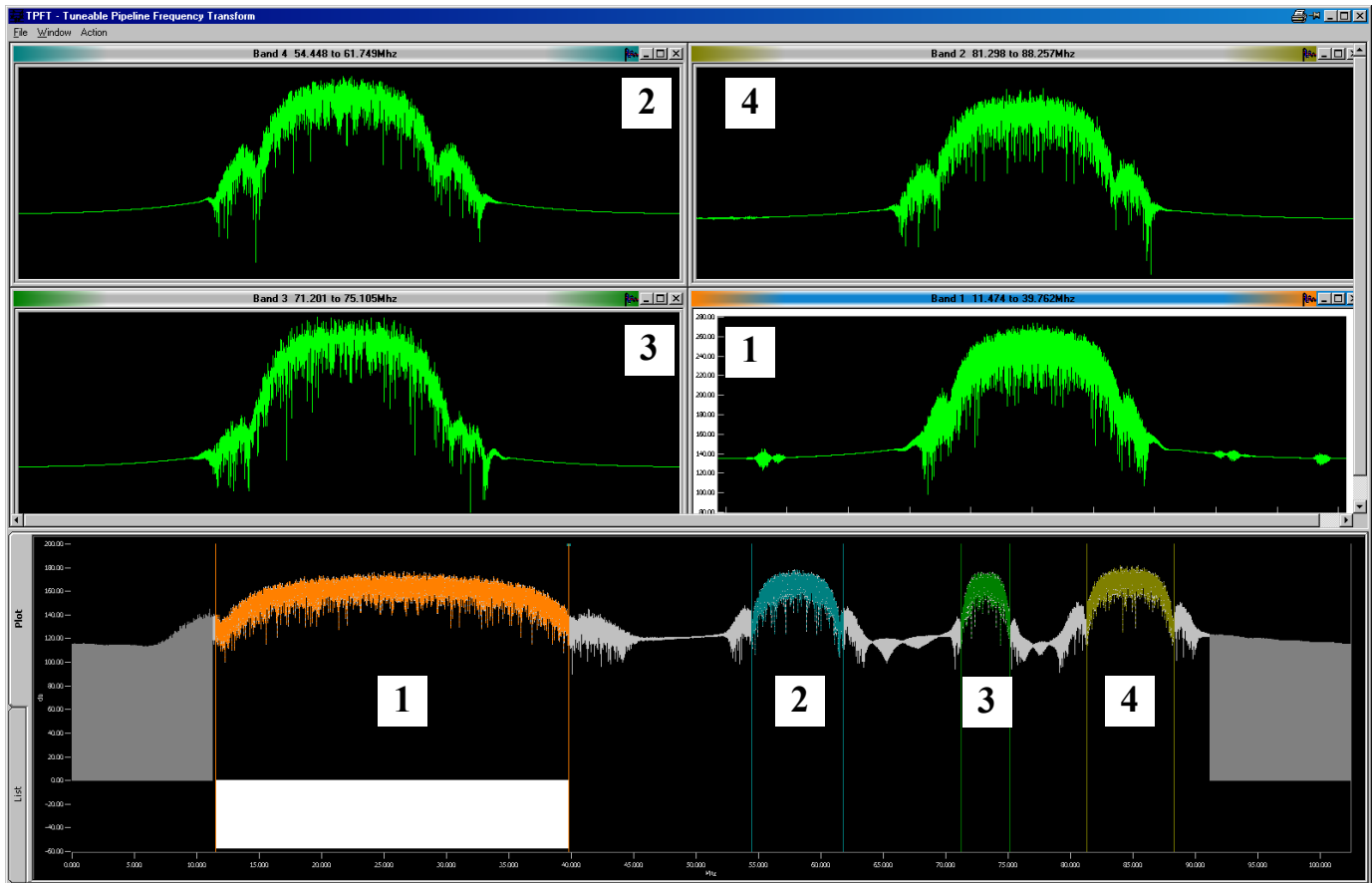


Figure 1 – Snap-shot of TPFT control software. The four extracted channels appear at the top half of the screen, whilst the bottom half represents the input spectrum.

The TPFT has been developed as an alternative to standard Digital Down Converters (DDC) techniques and offers significant advantages in terms of silicon utilisation. The architecture is highly pipelined, thus it is best suited to target devices such as FPGA or ASIC. The latest generation of the FPGA devices from the likes of Xilinx, Altera, etc. allows very complex DSP architectures such as the TPFT, to be implemented on single mid-range FPGAs. Furthermore, with the introduction of System on Chip (SoC) capable devices (e.g. Xilinx Virtex-II PRO), the whole system, i.e. filter bank and controls, can be implemented on a stand-alone platform.

A typical TPFT implementation would consist of 10 pipelined stages, providing in excess of 800 usable frequency channels at the finest frequency resolution (in this case a 1024<sup>th</sup> of the input bandwidth) or fewer channels if wider frequency bins are also required.

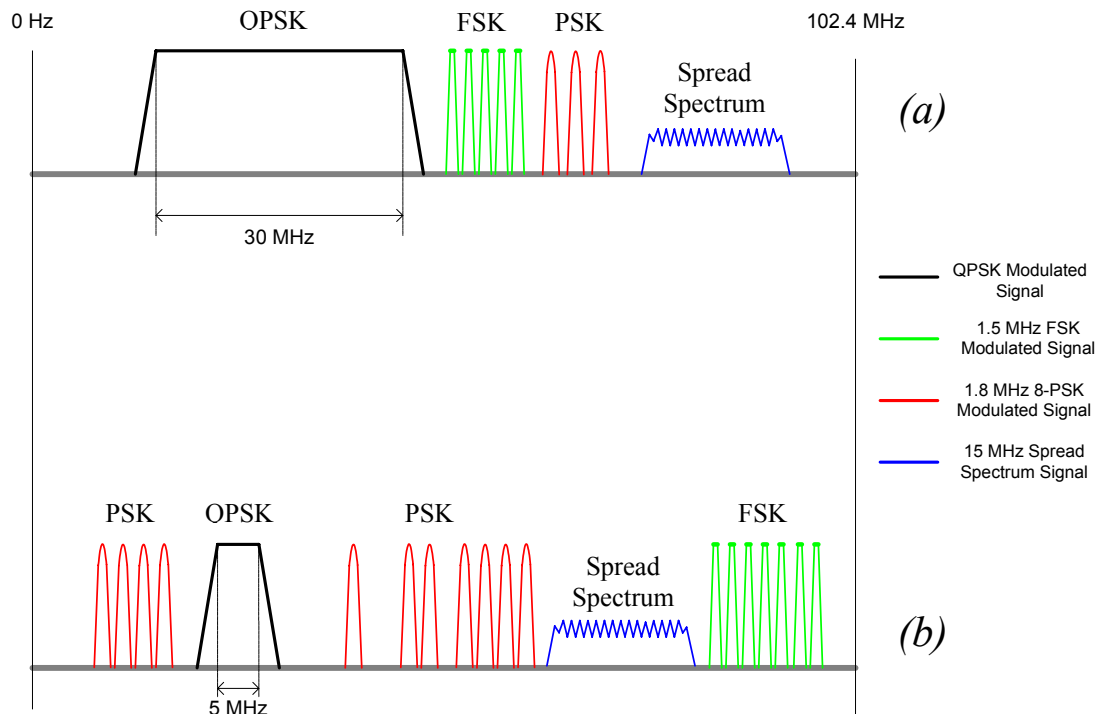


Figure 2 – Example of different frequency plans that the TPFT can switch between.

A hypothetical frequency plan is shown in Figure 2a. The TPFT can be configured to the plan and can extract the channels as shown. This frequency plan might change at some point in time to the one shown in figure 2b. If the new channels' positions and bandwidths are known in advance, then these can be input to the system and the TPFT control engine will automatically reconfigure itself to extract the new channels from the input spectrum.

The TPFT can be customised to accommodate for customers needs, leading to optimal tailored solutions: a TPFT design could perhaps compromise on tuneability where a frequency plan is fixed, leading to an even more compact implementation.

For the real-time processing of uneven channels and for on-the-fly reconfiguration, the TPFT architecture provides significant advantages over more conventional methods of frequency splitting, such as complex down converters, or even less flexible frequency transforms such as the Discrete Fourier Transform (DFT), etc.

Overall, the TPFT fills the gap between the comparatively inflexible FFT or PFT approaches and the use of DDCs, which is extremely flexible but becomes increasingly inefficient above a certain number of channels. The TPFT provides a highly flexible and efficient means of frequency channelisation, which is fully re-configurable within its hardware frame.

A software model of the TPFT is available for system engineers.

## RF Engines

RF Engines Limited (RFEL) is a UK based designer of high specification signal processing cores, sold as intellectual property (IP) for inclusion in SoC and semiconductor devices in the defence, communications and instrumentation markets. More specifically it is a solutions provider for projects requiring complex front end, real time, wide and narrow band, flexible channelisation. RFEL provides a range of standard cores covering multiple FFT and unique PFT techniques, as well as design services for specialist applications.

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