



RF Engines Ltd,
Innovation Centre
St Cross Business Park
Newport
Isle of Wight
PO30 5WB
Tel +44 (0)1983 550330
Fax +44 (0)1983 550340
E-Mail Info@rfel.com

RF Engines launches radical new way to simultaneously process digital signals across a wide bandwidth in real time

Patented architecture combines DSP, FFT, digital down converters and FIR filters for improved frequency transformation

RF Engines Limited, a British high technology company based on the Isle of Wight, has created a new way of simultaneously processing digital signals across a wide spectrum in real time. Following the successful business models of ARM, MIPS and Parthus, RF Engines is making this innovative architecture available as licensable Intellectual Property (IP) in the form of IP cores (or ‘engines’) that can be included in programmable logic devices or System On Chip (SOC) designs.

It enables a stack of Digital Frequency Converters or a massively parallel processed pipeline FFT to be replaced with a single chip, thereby reducing overall system cost and power consumption by up to 50%, whilst significantly improving performance. The key areas for its use are in broad bandwidth applications of up to 100MHz, such as the next generation of mobile phone basestations, spectrum analysers, radar and electronic surveillance equipment, that require conversion and filtering of channels (from a few to many thousand) in real time with all channel signals being available for onward processing.

“As this is a hardware implementation rather than software running on a programmable DSP,” explains John Lillington, RF Engines’ CTO, “we achieve up to twenty times better performance in high end applications. In fact, PFT makes possible a solution to high-end problems that was not practical before, due to the cost and size of silicon needed for conventional methods. For example, it would take a huge number of Digital Frequency Converters and filters or 86 GMACs on a programmable DSP with a total memory band width of 78 Gbytes/sec, which is not very practical, to match the performance of a 10 stage PFT producing a 1024 point output with a usable bandwidth of 80MHz. Each bin is equivalent to a digital downconverter followed by a decimate-by-64 CIC and a 67 Tap FIR filter with a 75dB stopband rejection.”

The **Pipelined Frequency Transform™** is a specially developed architecture that is optimised for the real time signal analysis of ultra wideband signals and transforms the signals from the time domain to the frequency domain as an FFT (Fast Fourier Transform) would do. However, unlike an FFT, the PFT also provides high performance filtering across hundreds of channels. This could not be done practically in real time on a general purpose DSP running FFT routines.

For example, a demonstration implementation of PFT on four FPGAs can handle in excess of 100MHz bandwidth signal at 8-bit resolution and extract 1,024 channels with sharp channel filter characteristics of, typically, a filter stop-band rejection of better than 75dB (with 8 bit A/D data input). Moreover, it can do a 1024-point transform up to 20 times faster than an FFT implemented on a DSP. The basic PFT architecture uses a series of frequency splitting stages to sub-divide the original signal band. The first stage splits the band in half; the second splits the two bands into four, and so on until the required number of bins is achieved. Decimation at each stage ensures a constant data rate through the pipeline, and hence a continuous data throughput with no loss of data. Gain across each bin is flat (typically less than +/- 0.2 dB) and bin-to-bin isolation can be tailored using highly optimised filters within each stage to meet the dynamic range requirements of the system.

An N-point PFT is functionally equivalent to a parallel bank of N individual complex down-converters; i.e. all frequency channels are available all of the time. For large values of N, the PFT solution requires significantly less silicon than the equivalent bank of down-converters. Thus, for example, a 16K point transform needs only 14 PFT stages as compared to 16384 Digital Frequency Converter modules.

The architecture is totally scaleable with intermediate stage outputs simultaneously available if required. It is configurable so that trade-offs between dynamic range, selectivity, throughput rate and silicon gate requirements can be done under the designer's control to provide the optimal solution for each application.

Being pipelined means that there are no time gaps and therefore no missed data, which is crucial for very fast or fleeting signals. In addition, it is completely cascadable by adding additional PFT stages to provide higher resolution by increasing the number of points or, conversely, finer resolutions can be achieved if a smaller input bandwidth is used.

Furthermore, and of major significance, the PFT can also be tuned to allow flexible dynamic channelisation of broadband spectrum without affecting static channels during the reconfiguration process.

Two examples of typical PFT designs

1) High bandwidth medium resolution project.

This project is required to continuously monitor an entire 80MHz band with a resolution <100KHz, an update rate >200KHz, a dynamic range >75dB and across-bin ripple <0.1dB.

A PFT based implementation could be achieved as follows: *80MHz wide signal centred 51.2MHz IF, sampled by an 8-bit ADC sampling at 204.8MHz, followed by a digital half-band filter, I and Q data rate of 102.4MHz, followed by a 10-stage PFT with the required bin shape, giving 1024 bins each of 100KHz wide and a continuous update rate of 200KHz.* All the digital hardware fits within a single XCV3200E Xilinx Virtex-E FPGA (3.2 million gate part, 35mm x 35mm).

For comparison, an FFT based implementation would require at least four overlapping 4K-point weighted FFTs running in real time at 102.4Msamples/s to meet all requirements of the project. This would clearly require vast quantities of processing power and data path bandwidth compared with the single chip PFT solution.

2) Medium bandwidth high resolution project.

This project is required to continuously monitor an entire 4MHz band with a resolution <200Hz, an update rate >200Hz, a dynamic range >130dB and across-bin ripple <0.2dB.

A PFT based implementation could be achieved as follows: *A high dynamic range ADC sampling at 10.24 MHz, followed by a digital half-band filter with an output data rate of 5.12MHz, followed by a 15-stage PFT giving 32K bins each of 156.25Hz wide and a continuous update rate of 312.5Hz.* All digital hardware fits within two XCV2000E Xilinx Virtex-E FPGA (2 million gate parts) and eight external RAM devices.

For comparison, an FFT based implementation would require at least eight overlapping 256K-point weighted FFTs running in real time at 5.12Msamples/s to meet all requirements of the project. Again, a huge processing task compared with the PFT solution.

For further information, please see the website at www.rfel.com or contact RF Engines at Innovation Centre, St Cross Business Park, Newport, Isle of Wight, PO30 5WB, Great Britain. Tel +44 (0) 1983 550330. E-mail info@rfel.com.

Press information and illustrations can be obtained from Nigel Robson, Vortex PR, Island House, Forest Road, Guernsey, GY8 0AB, Great Britain. Tel +44 (0) 1481 233080. E-mail nigel@vortexpr.com.

All trademarks are the property of their respective owners.