

**Introduction to RFEL and the new
Pipelined Frequency Transform (PFT™) Technology**



RF Engines Ltd.(RFEL) is an Intellectual Property company. It is a leading designer and developer of novel core architectures for the programmable logic (hardware) and ASIC industry. RFEL's principal offices are located on the Isle of Wight, off the south coast of England.

The Company was established in 1999. It evolved as a business unit of the Libra Design Associates Consultancy, which specialised in digital signal processing designs for the communications and instrumentation industries. Libra's digital expertise was in the area of Fast Fourier Transforms, Finite Impulse Response filters and analysis of RF signals. Libra also provided RF and microwave design services for the communications and instrumentation industries.

Building upon this experience, RFEL was established to accelerate the development of a radical new technology in the areas of wide band real time frequency analysis and multi-channel digital frequency converters. The RFEL core IP blocks provide significant advantages over other available techniques, and allow system designers a faster route to market.



The Problem

Analogue to digital converters (A/D's) to beyond 1Gs/s are commercially available but real-time data processing beyond 100Ms/s is very difficult and expensive. Parallel programmable DSP processing is required for more complex applications especially where fine resolution is required.

To achieve the high throughput rate of the PFT, with complex data streams typically exceeding 100Ms/s, it is necessary to use distributed hardware processing. In addition to the obvious speed advantage of such an approach over programmable DSP, the PFT is an architecture which makes extremely efficient use of silicon and avoids the need for traditional multiply / accumulate (MAC) processes.

The PFT is being demonstrated through programmable logic but it is not limited to such a technology. The flexible architecture can also be implemented in ASIC or future technology devices such as system programmable devices.

What is the PFT

The Pipelined Frequency Transform (PFT) is a special purpose piece of hardware, which carries out the function of a multiple stack of Digital Frequency Converters, which provide conversion and filtering of channels within a spectrum bandwidth of up to 100MHz. This function is carried out in real time (at the A/D clock rate) with all channels available for onward processing.

This core will be applicable where a wide band spectrum needs to be channelised and the number of individual frequency converters would be prohibitive. An alternative use is as a replacement for the traditional FFT, providing vastly improved frequency 'bin' selectivity and flatness as well as real-time pipelined processing.

The PFT can be supplied as firm or hard IP, depending on the application and performance requirements. It is also envisaged that the core will be parameterised to enable fine-tuning of the hardware design for specific applications.

The PFT is a completely novel approach to frequency transformation. Using patented architecture it has the following advantages over the FFT approach: -

- **Much Sharper Filter Response**
- **Very Flat Response Across Frequency 'Bin'**
- **Very Fast**
- **Pipelined = No Gaps in Time = no Missed Data**
- **Completely Cascadable (for higher resolution)**
- **Architecture Ideally Suited to FPGAs & ASICs**
- **Simultaneous PFTs of Different Sizes Available**
- **Provides Multi Channel Digital Downconverter**

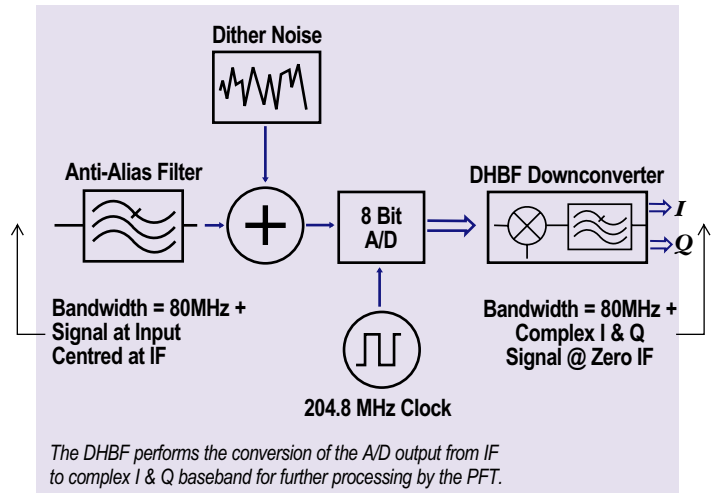
The PFT is a radically different technique from the FFT and pipelined FFT. The PFT will take information from an analogue to digital converter (A/D) with an effective spectrum bandwidth of up to 100MHz. It will provide real time processing without any gaps in time to produce a 1024 point transform. Higher and lower point transforms can be achieved. With an FFT it is difficult to realise a flat frequency response across a 'bin' whilst maintaining good isolation of adjacent frequency 'bins'. The individual bin filter performance of the PFT far exceeds that available from any other type of process in real time. Typical filter stop-band rejection is better than 75dB (with 8 bit A/D data input). There is a trade-off between dynamic range, selectivity, throughput rate and silicon gate requirements, that are all under the designers control.



The Input Distributed Half Band Filter (DHBF)

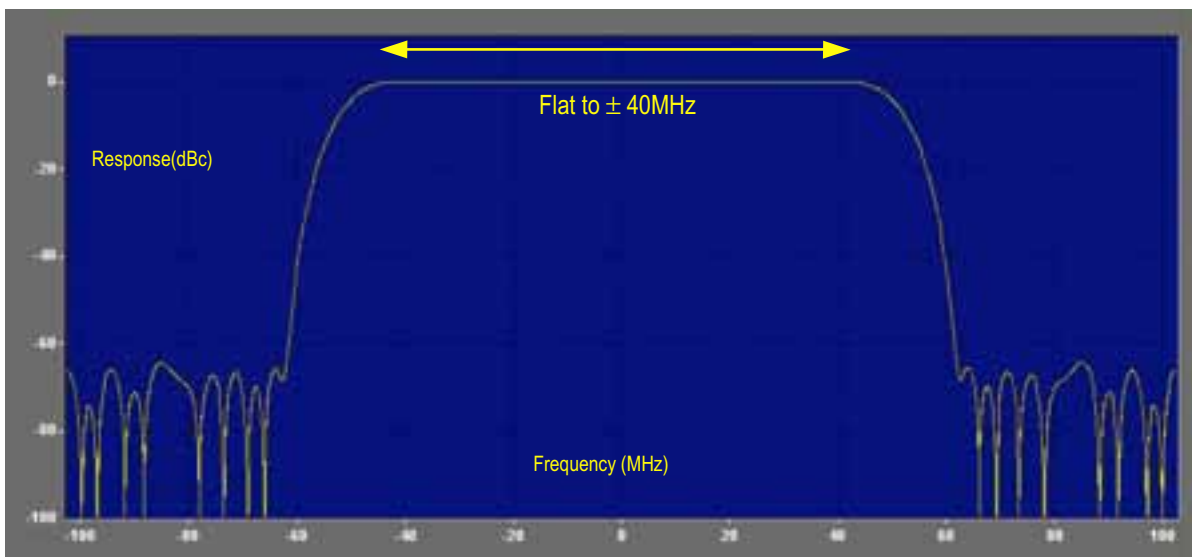
The PFT function can accept data that has already been downconverted to complex baseband I & Q, or the DHBF can be provided as part of the RFEL IP. The DHBF allows very fast processing by the use of a unique distributed filter architecture which allows extremely wideband (up to 100MHz) block downconversion to complex baseband I & Q.

In the RFEL demonstration system, the input to the PFT board is in the form of two 8 Bit PECL outputs from the A/D, representing odd and even samples. The PFT IP will accept inputs from A/Ds running up to 16 bit coding. Thus the PFT can be easily tailored to meet with a range of A/D outputs for different applications. The maximum A/D clock rate that can be used is approximately 200 MHz, although higher speed architectures are being developed. It is critical that the response of the DHBF or other form of block downconverter has a flat frequency response to provide optimum performance.



Typical Front End Configuration for Feeding the PFT Function

RFEL Typical DHBF Filter Response



Another useful feature of the DHBF is the Undersampling Mode which allows sampling of a series of (e.g.) 80 MHz bands up to the A/D analogue input bandwidth.

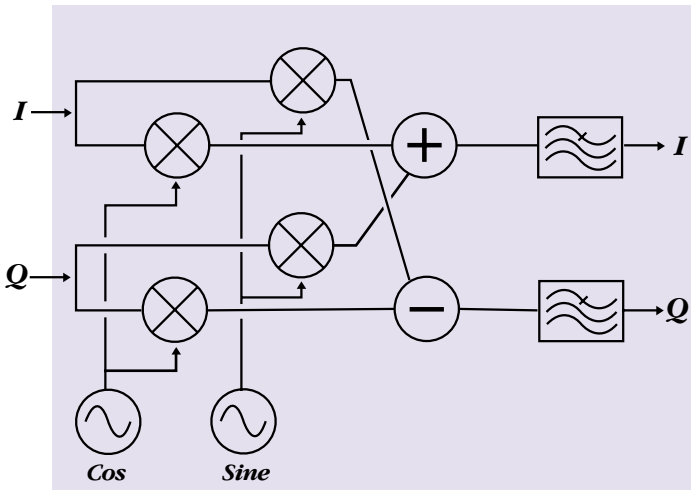
Example: Sample Rate = 204.8 MHz

Possible Sampled Bands Are:

Normal	Inverted
11.2 - 91.2 MHz	113.6 - 193.6 MHz
216.0 - 296.0 MHz	318.4 - 398.4 MHz
420.8 - 500.8 MHz	523.2 - 603.2 MHz
625.6 - 705.6 MHz	728.0 - 808.0 MHz
830.4 - 910.4 MHz	932.8 - 1012.8 MHz

These bands will of course be subject to degraded spur and noise floor performance but could obviate the need for expensive RF front end tuning in certain applications.

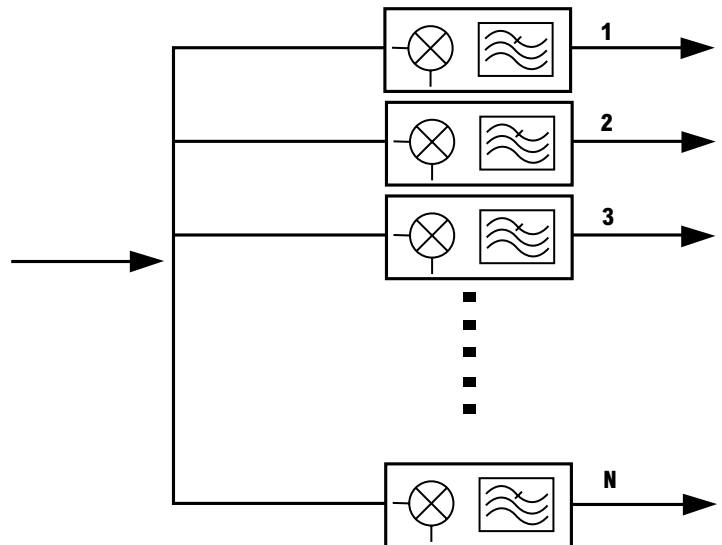
The PFT itself



Standard form of complex downconverter / filter i.e. Passband to I & Q baseband.

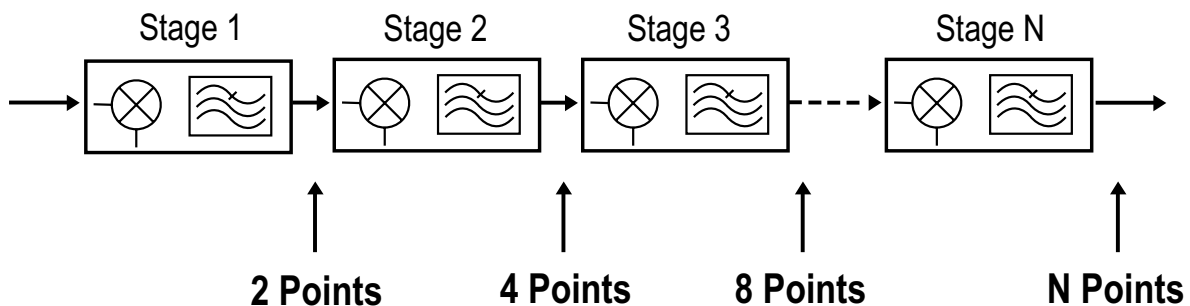
The figure above shows the standard form for a complex frequency converter, requiring sine and cosine local oscillators (typically look-up tables), four multipliers, two add / subtracts and two low-pass filters. This architecture is similar for either up or down-conversion.

Multiple Stack of Digital Frequency Converters



To provide an equivalent function to the PFT using standard techniques, N-off complex converter/filter modules are required as above. e.g. a 16K point transform requires 16384 modules. This is obviously not an efficient use of silicon. An FFT or pipelined FFT could carry out a similar function but would provide greatly inferior filter performance.

The PFT Architecture

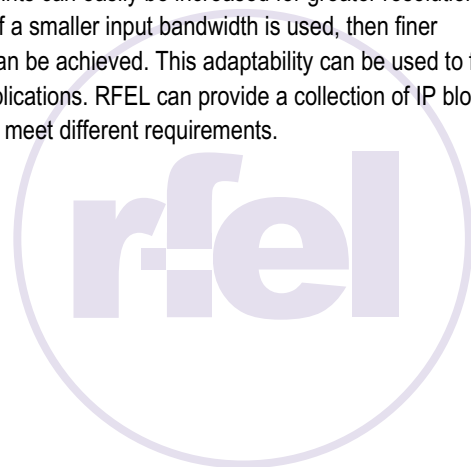


The PFT is equivalent to the Multiple Stack of Digital Frequency Converters diagram above but uses a novel patented architecture, which is ideally suited to FPGAs and uses significantly less silicon.

The PFT N-Point Transform only requires $\log_2(N)$ Complex Downconverter / Filter stages.

For a 1024 point Transform, only 10 stages are required. A 16K point Transform needs only 14 stages. Obviously the individual PFT of stages are more complex than a simple frequency converter but are still extremely efficient in higher point applications or where Fourier Transform filter shape is not good enough for the application.

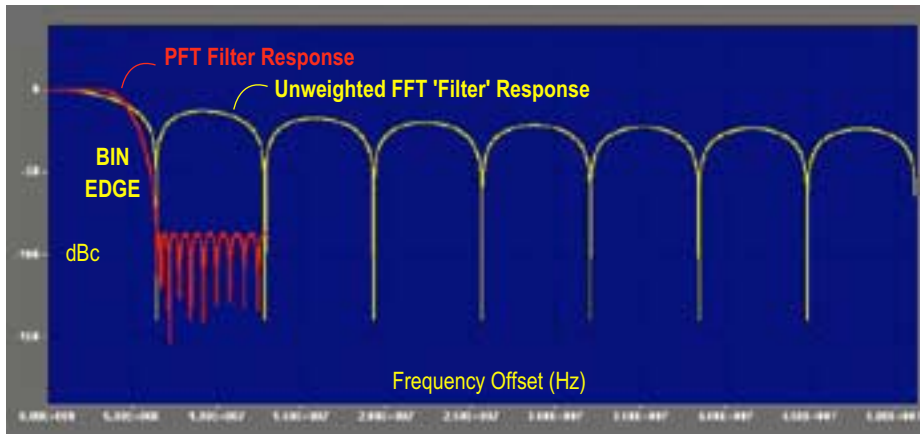
The PFT architecture means that with the addition of silicon, the number of points can easily be increased for greater resolution. Conversely, if a smaller input bandwidth is used, then finer resolutions can be achieved. This adaptability can be used to fit a variety of applications. RFEL can provide a collection of IP blocks configured to meet different requirements.



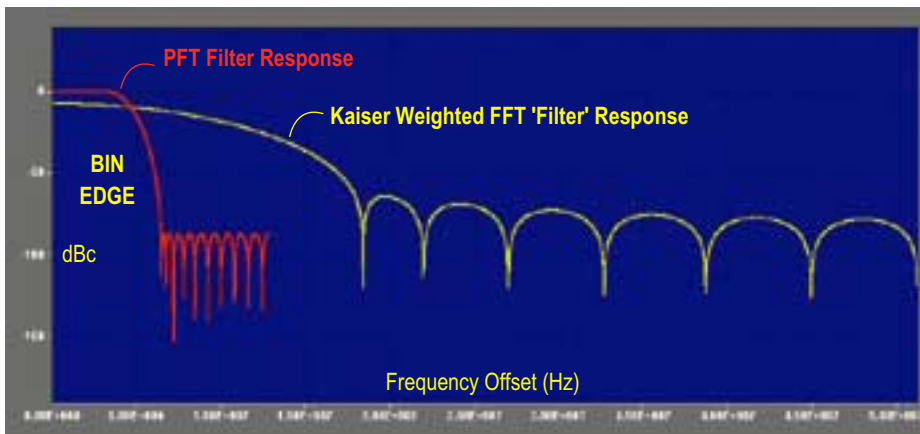
PFT Filter Response

The PFT overcomes the need for windowing as used in traditional FFT techniques as the data is processed continuously with built in filters. This feature yields a much sharper filter response and a very flat response across the frequency bin. This in turn provides

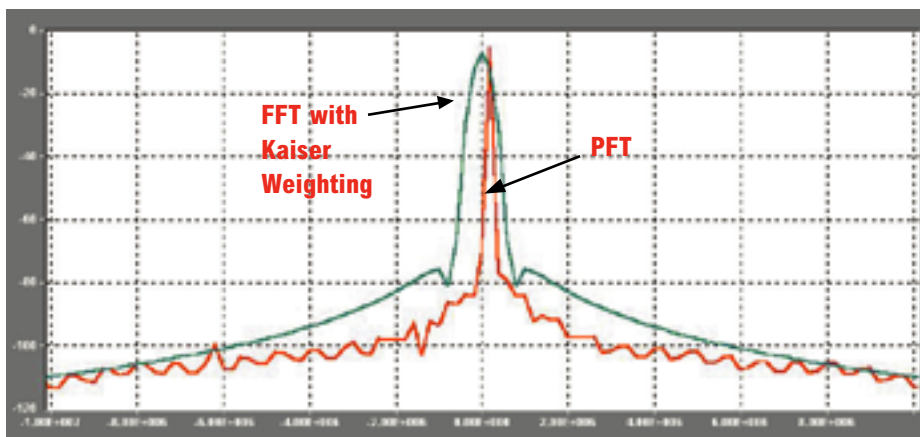
excellent selectivity and dynamic range, which will ultimately increase performance in spectral analysis applications and allow multiple narrow channels to be selected (downconverted) from the broader spectrum.



Comparison of Typical PFT Filter and Unweighted FFT



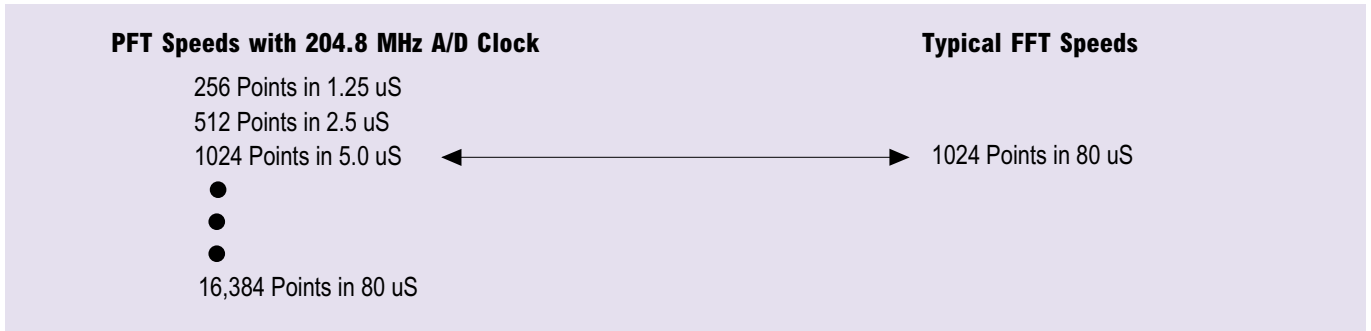
Comparison of Typical PFT Filter and Kaiser Weighted FFT



Signal Comparison of 512 Point Transforms for CW Signal

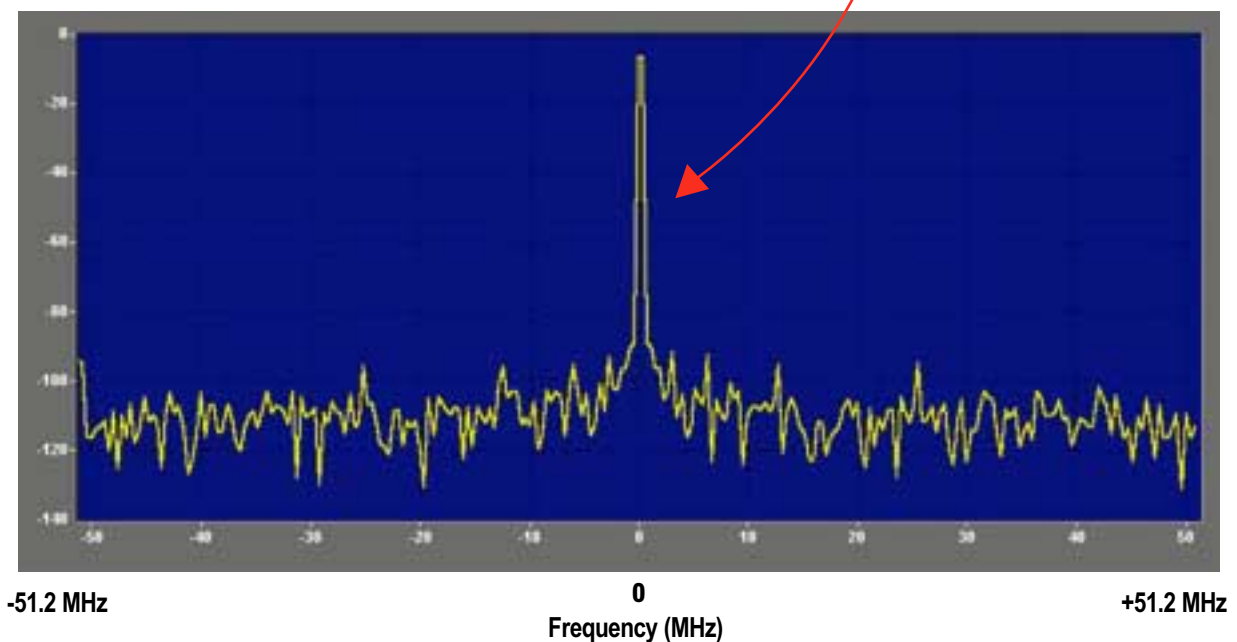
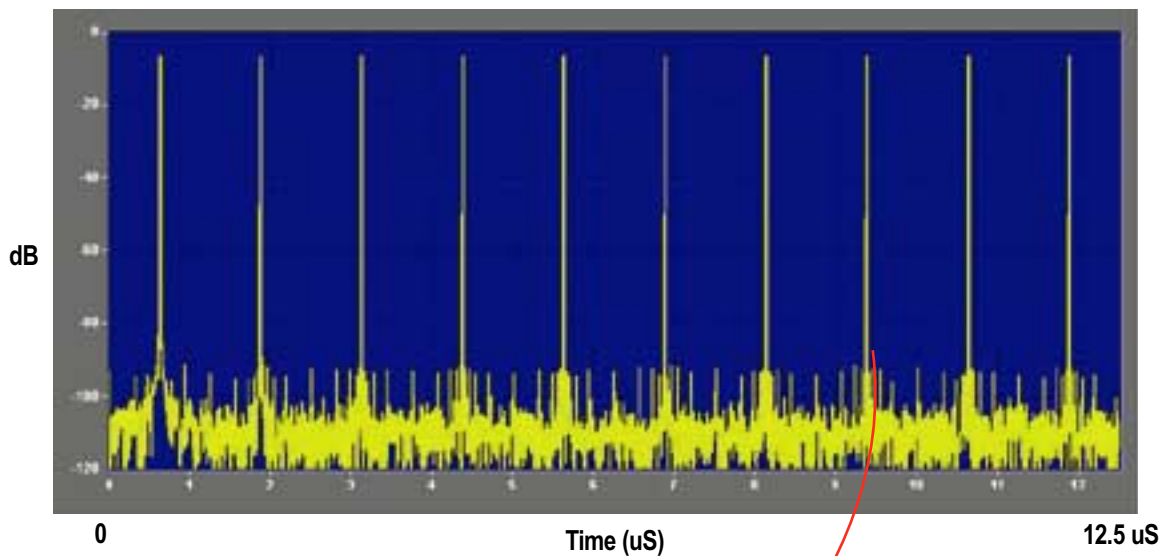
The PFT Speed of operation

The PFT is extremely fast when compared to an equivalent FFT implemented in a fast programmable DSP. The PFT is up to 20 times faster than the equivalent FFT implemented in a state-of-the-art DSP.



The diagrams below show 10 consecutive 256 bin transforms and a single 256 bin PFT in more detail. With an A/D clock of 204.8 MHz a single PFT represents a frequency span of ± 51.2 MHz.

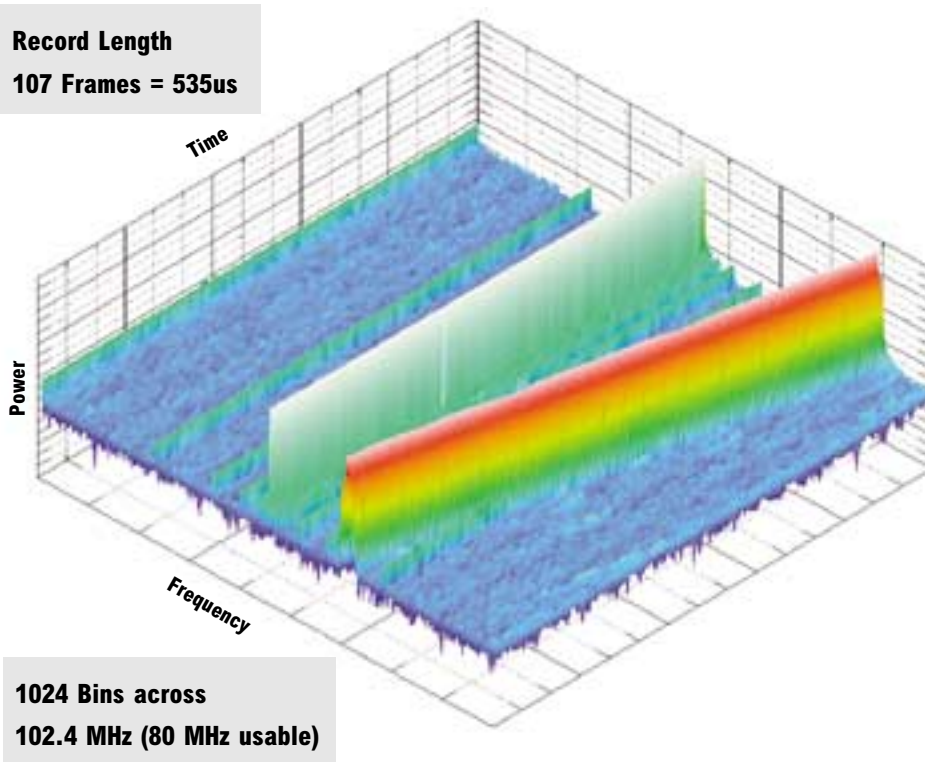
Example :- 10 - off 256 Bin Transforms in 12.5 μ S (= 1 Transform in 1.25 μ S)



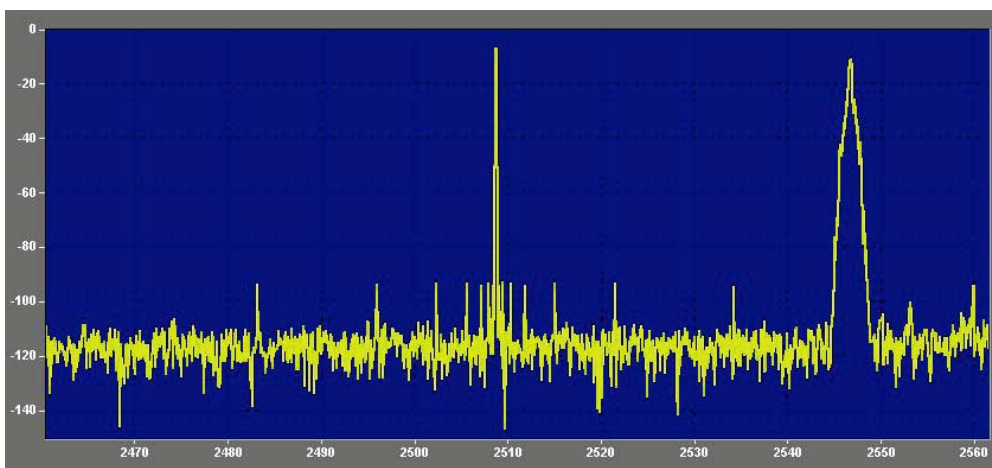
1024 Point Transforms of CW + Signal Tracking @ 40 GHz/s

The Pipeline Processing means there will be no gaps in the data which will enable the tracking of very fast or fleeting signals. The waterfall plot below gives an example of a stable CW signal at the

centre of the frequency band and another tracking CW signal. In this example the tracking signal is moving at 40GHz a second but can still be clearly identified.



The spectral picture of a single frame is shown below.



Single Transform RBW = 100 kHz

Architecture suited to FPGA's and ASIC

Standard DSP based FFTs are not well suited to FPGAs as the intermediate data results need to be written to, and from memory. However the PFT is well suited, due to the pipelined flow of data from input to output with no addressable memory required. The process involved uses fixed shifts, adds and delays with no need for complex multiplication.

Although the PFT has been implemented, for convenience, using FPGAs, the architecture is equally suited to ASICs. This would result in reduced silicon requirements for a given performance, but with loss of flexibility.

Availability of Simultaneous PFT.

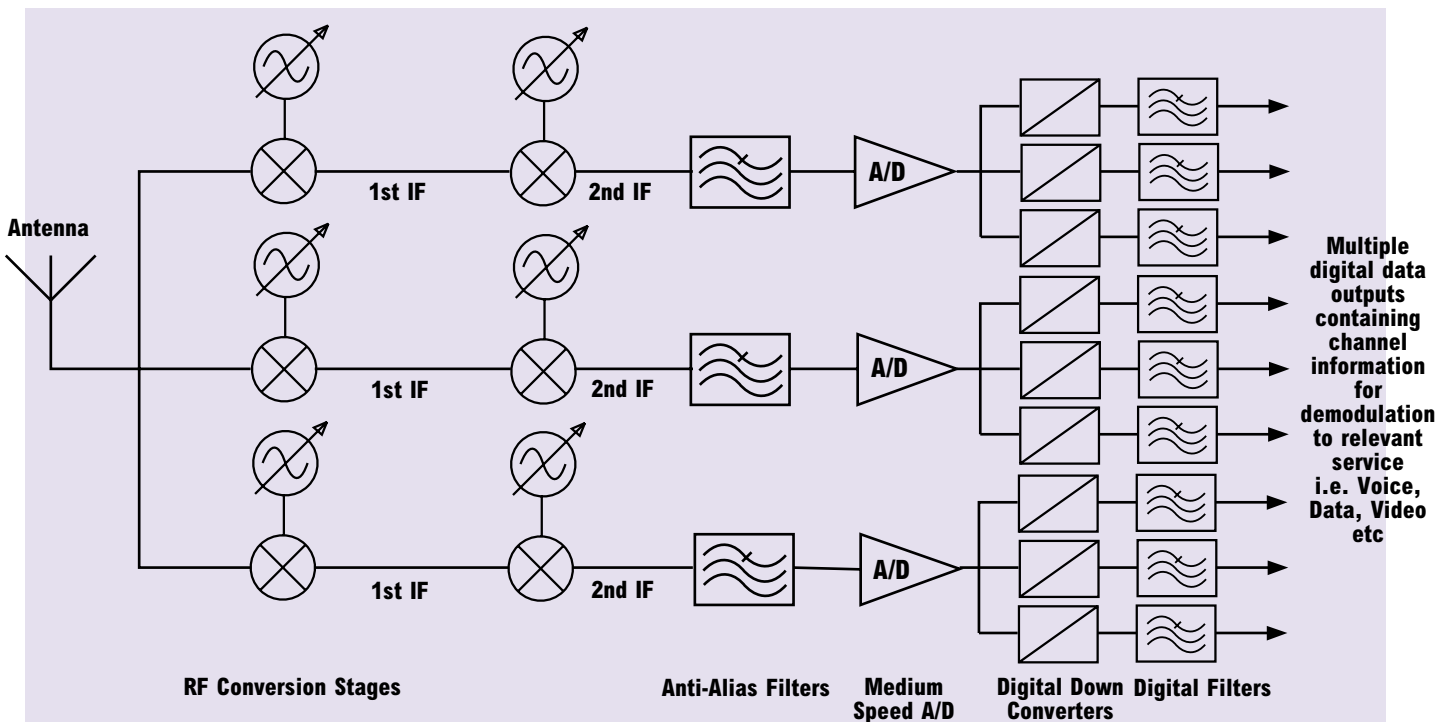
By placing auxiliary outputs between the different stages of the PFT it is possible to output PFTs with a different number of points and different Resolution Bandwidths (RBWs) simultaneously. For example a 256 point PFT with 400 kHz RBW can be output at the same time as a 16K point Transform with 6.25 kHz RBW.

This feature, as shown in the diagram overpage, is useful for catching fleeting signals in the wider RBW with a faster update time. It could also be useful for selecting signals of different bandwidths for further processing.

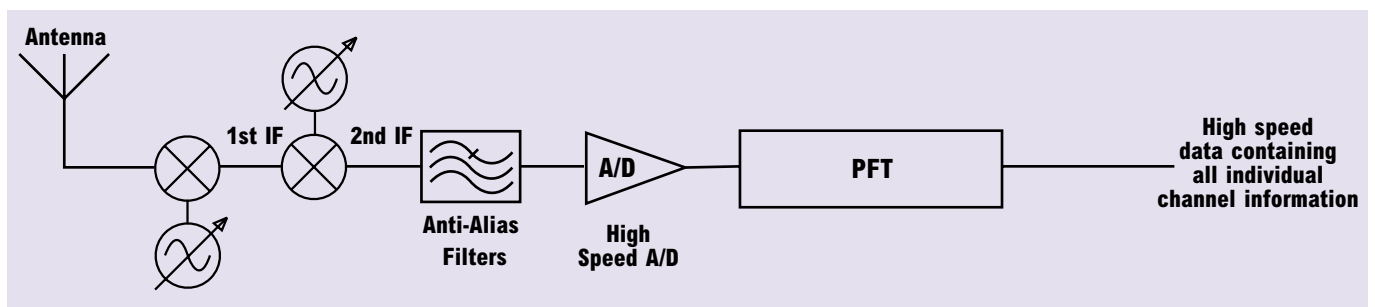
PFT as a multi-channel digital downconverter

By programming the system to only output relevant bin information, the PFT can be used to provide wideband multichannel downconversion in realtime allowing a multichannel receiver to be configured, perhaps even dynamically.

Below is a typical example of a multi-channel digital downconverter. The input RF bandwidth is too wide to be dealt with by one single RF chain and A/D processing section.



However, the equivalent PFT design would be as below, possibly providing significant savings in silicon and improved performance.



RFEL's IP Implementation

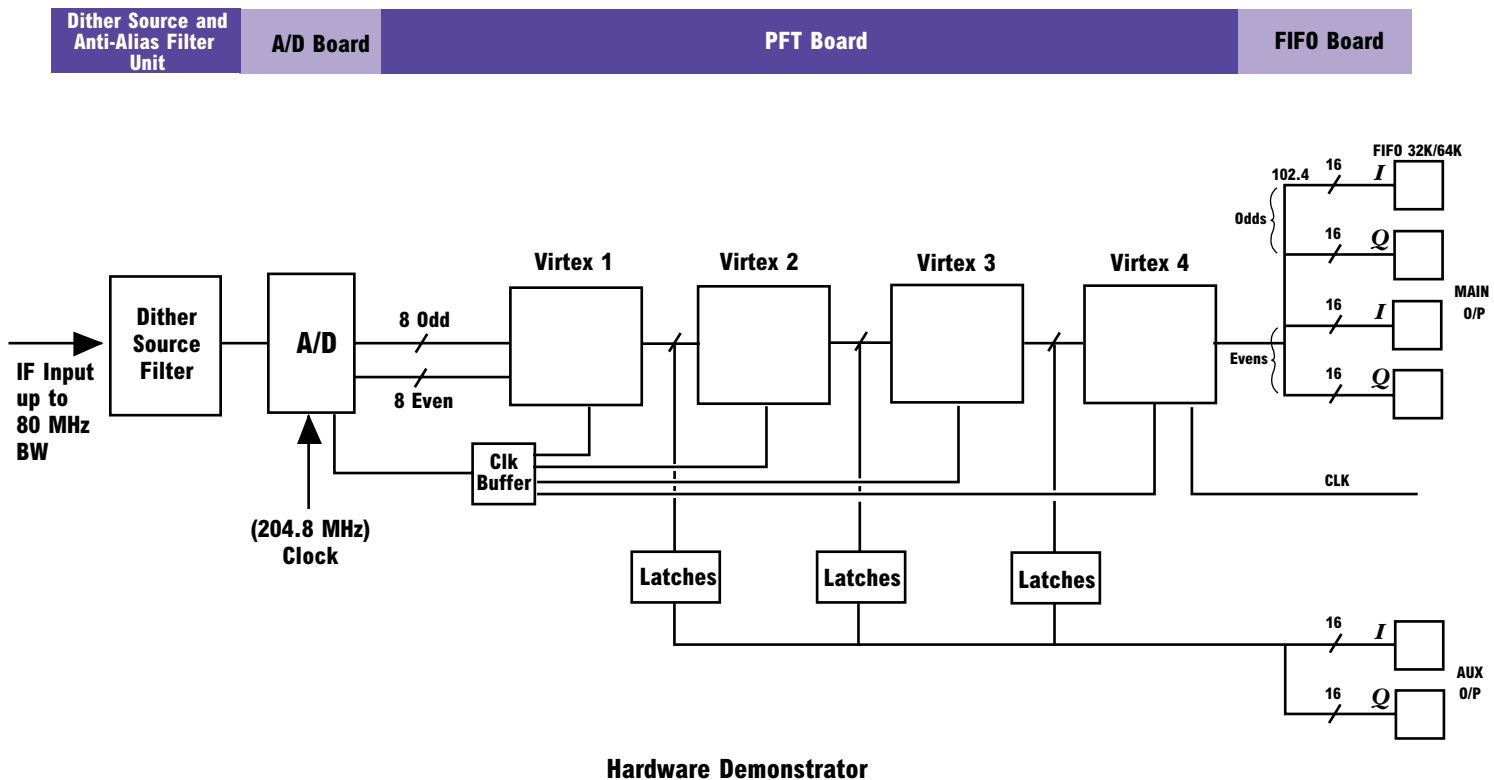
The PFT is supplied as IP currently for use on Xilinx-VirtexE FPGAs, and is being configured for future Virtex II devices. Portability to other FPGAs, such as Altera, is possible as is design into ASIC. RFEL uses a wide range of design tools including : Modelsim, Xilinx Foundation, Leonardo Spectrum, Matlab-Simulink and Elanix-SystemView to ensure optimum performance and reduced design time.

The diagram below shows how the RFEL hardware demonstration unit has been constructed using 4 Virtex 1000E FPGAs. The input signal is passed through an anti-alias filter and then dither noise is added before A/D conversion takes place in an 8 bit Maxim chip running at up to 204.8Ms/s. The odd and even samples in PECL format are then fed to the first FPGA which contains the DHBF. The FPGA clock source is also derived from the A/D board where it is conditioned in the clock buffer and distributed as necessary.

After the data is converted to baseband in the DHBF the PFT process begins. Each module or stage of the PFT will provide signal splitting with the effective resolution bandwidth being halved at each stage but with the full input bandwidth available at the output.

The hardware demonstrator will contain 1 DHBF and 10 PFT stages providing a 1024 point conversion of the input signal. The output data is in the form of 4 X 16 bit outputs at 102.4Mhz representing odd and even samples for onward processing. For demonstration, RFEL has provided a 64k FIFO board with a USB interface board to gain access to the data.

In addition to the main output after the 10th Stage, an auxillary output could be selected from any stage along the PFT process.



To summarise the main benefits of the PFT.

- **Filter Response Provides Improved Selectivity**
- **Very Flat Response Across Frequency 'Bin' Increases Accuracy**
- **Fast Processing Speed for Detection of Transient Signals**
- **Pipelined Approach = No Gaps in Time = No Missed Data**
- **Scalable for Various Applications**
- **Adaptable Architecture Ideally Suited to FPGAs & ASICs**
- **Simultaneous PFTs of Different Sizes Available for Multi Role Applications**



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