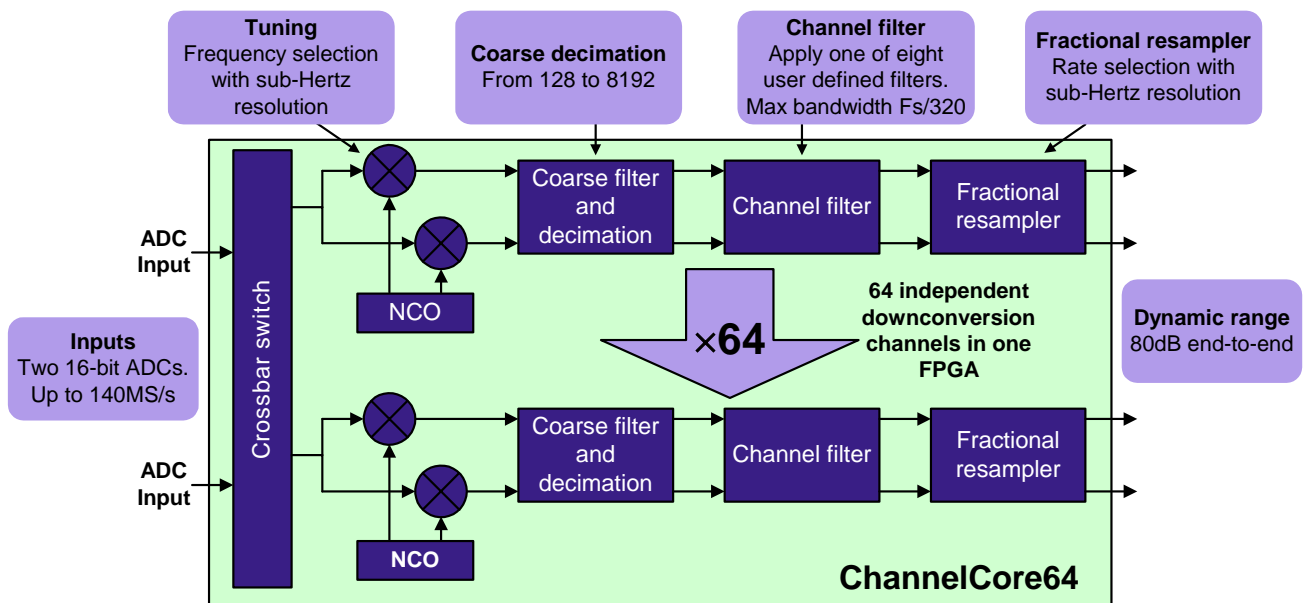


ChannelCore64

64 Flexible DDC Channels in one FPGA

ChannelCore64 allows designers to replace up to 16 specialist 4-channel DDC ASIC devices with a single IP core for FPGA, significantly reducing board area, lowering power consumption, and increasing flexibility. The new approach represents a major cost saving over traditional methods, with savings becoming more significant as the number of channels increases. ChannelCore64 is targeted at applications such as wireless base stations, satellite ground stations, and other multi-channel radio receivers.



ChannelCore64 Functional Representation

Features

- 64 independent down-conversion channels
- Support for two 16-bit ADC inputs up to 140MS/s
- Alias free channel bandwidths, up to 437.5 kHz
- Independent tuning of channel centre frequencies with resolution of <math><0.01\text{Hz}</math>
- Select output rates with a resolution of <math><0.01\text{ Hz}</math>, up to 1.09 MS/s
- Reconfigure channels without affecting operation of other channels
- End-to-end dynamic range of 80dB
- Gain control

Benefits

- Fits within a single Xilinx Virtex II Pro 30
- Replaces up to 16 four-channel DDC ASICs
- At least 8 times more silicon efficient than standard DDC cores
- Bit-true Matlab models for system simulations
- Custom versions available optimised to application

Applications

- Telecommunications base stations
- Satellite ground stations
- Software defined radio
- MIMO receivers

FPGA Resource Requirement

ChannelCore64 is designed for use with Xilinx Virtex II Pro FPGA devices. The FPGA resource requirements are presented in the table below. Variants of the core can be provided for other FPGA families including Xilinx Virtex 4 and Altera Stratix II.

	Block RAMs	Multipliers	Logic slices
Xilinx Virtex II Pro	84	81	11437
Proportion of XC2VP30	62%	60%	84%

Power Consumption

FPGA : Xilinx Virtex II Pro 30	Power
Typical power consumption with all channels active	4W

Deliverables

ChannelCore64 is delivered with the following items

- Design [EDIF Netlist]
- User Constraints File
- Instantiation Template
- VHDL model and Test Bench
- Matlab model

Licensing

ChannelCore64 is provided under a simple licensing arrangement. For further details on latest pricing please contact info@rfel.com.

General Description

ChannelCore64 can be used for extracting up to 64 narrow band channels from one or two wideband ADC inputs. The core is based on a novel channelisation architecture, which provides the flexibility traditionally associated with DDC cores and ASIC devices, but with significantly greater silicon efficiency. The major functional blocks are:

Crossbar switch	Each channel may take its input from either ADC channel.
Frequency control	Each channel may have its frequency shift selected with any frequency in the range $0 - F_s$, where F_s is the sample rate of the ADC, with a resolution of $<0.01\text{Hz}$.
Filtering	Once shifted in frequency, each channel is filtered using one of eight user programmable low-pass filters. Filter shape is relative to sample rate, and hence each filter shape can provide a large number of possible output bandwidths.
Output sample rate control	A resampler provides output rate control for each channel to allow matching with modulation symbol rates. Sample rates may be selected with a resolution $<0.01\text{ Hz}$.
Gain control	A saturation level indication, and fine-level gain control with 0.01dB resolution is provided for each channel.

The core maintains an end-to-end dynamic range of at least 80dB including the output resampler stage.

Channels are completely independent and may be reconfigured without interrupting the flow of other channels.

Variants

RF Engines are able to quickly produce variants of the ChannelCore architecture to give an optimal channelisation solution for a specific requirement. This includes cores that support more or less channels, wider maximum bandwidths, or faster input sample rates. The associated up-conversion cores can also be provided upon request.

