



# Xilinx FFT Library

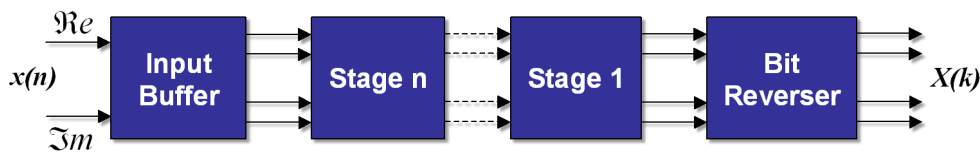
## Pipelined FFT Cores for Xilinx FPGA

### Product Information Sheet

RF Engines' FFT Library provides developers with a range of high performance Fast Fourier Transform (FFT) cores for Xilinx FPGA. The cores are designed to be highly silicon efficient and support complex sample rates up to 500 MHz. Therefore, through a suitable digital down-converter the core may be matched with analogue to digital converters with sample rates up to 1GHz.

The library includes more than sixty individual FFT netlists, and is based on RF Engines industry leading HiSpeed and QuadSpeed architectures. A wide range of FFT lengths are provided ranging from 32-point up to 32K-points. Furthermore, each core includes a bit-true Matlab model that can be used to precisely simulate the performance of the FFT reducing the risk of problems when implemented on the target device.

The FFT Library supports Xilinx Spartan III, Xilinx Virtex II, and Xilinx Virtex II Pro FPGA devices. Virtex 4 FPGA devices can also be targeted using the Virtex II Pro netlists supplied.



The FFT cores use pipelining techniques and parallelism

### Features

- Individually optimised for Xilinx Spartan III, Virtex II, and Virtex II Pro devices
- Virtex 4 support using Virtex II Pro netlists.
- Complex transform lengths from 32-points to 32K-points
- Optimised for two sample rate ranges:
  - HiSpeed: up to 100 MS/s complex
  - QuadSpeed: up to 500 MS/s complex
- Pipeline architecture allows continuous processing with no gaps in data
- Fully synchronous designs
- Use of fixed-point processing ensures optimal silicon usage
- Inverse FFT control input

### Benefits

Compared to FFT generation tools the FFT library offers:

- Higher real-time processing speed options
- More silicon efficient options for lower speeds
- Placed and routed designs with test benches for easy integration
- Bit –true Matlab models for system simulations
- Factory support
- Custom versions available optimised to application

### Applications

Wideband Spectral Analysis   ⊗  Frequency Domain Filter Banks   ⊗  Communication Systems  
 Defence Receivers and Signal Monitoring (RADAR, SONAR, surveillance)  
 Image Processing   ⊗  Medical and Scientific Instruments   ⊗  OFDM Systems

## FFT Architectures

The FFT library includes cores based on RF Engines HiSpeed and QuadSpeed architectures, both of which are pipelined implementations of the complex FFT algorithm. The QuadSpeed design has a higher level of parallelism when compared to the HiSpeed, thereby allowing it support higher sample rates but requiring additional silicon.

The HiSpeed and QuadSpeed FFT architectures are shown in Figure 1 and Figure 2 respectively.

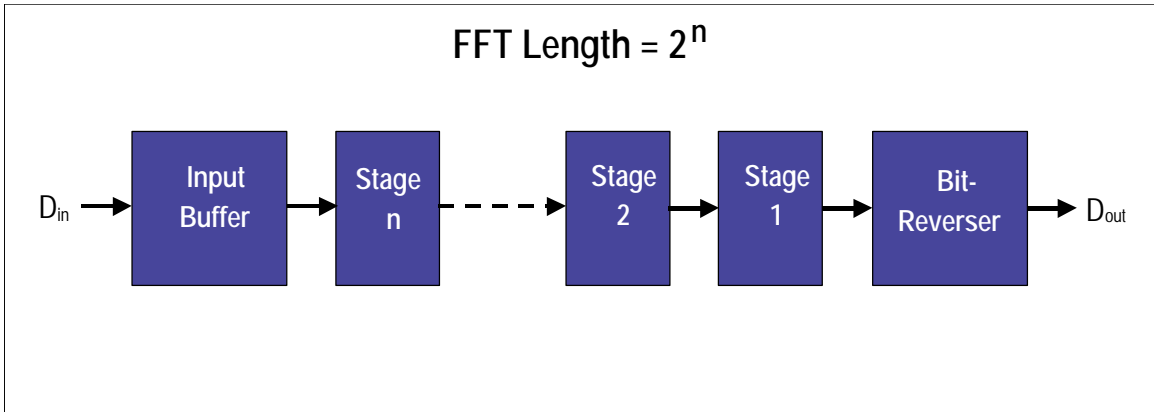


Figure 1: HiSpeed FFT Architecture

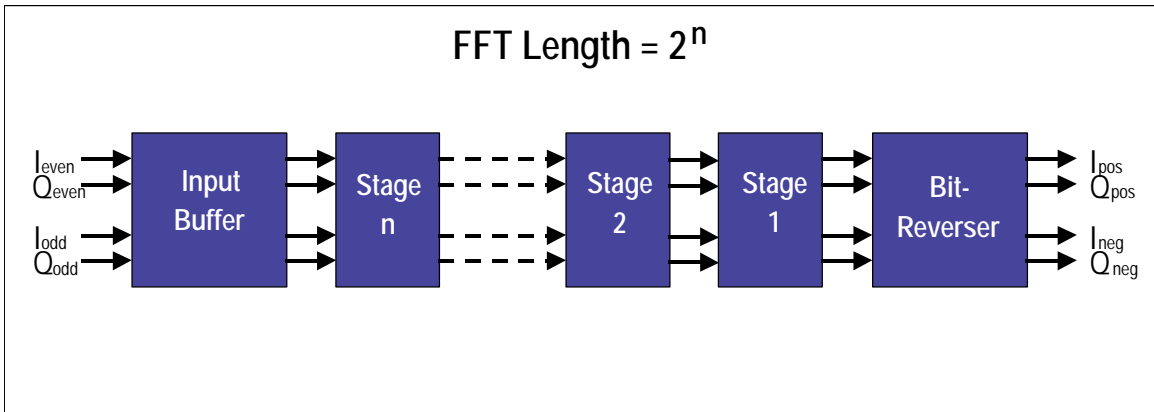


Figure 2: QuadSpeed FFT Architecture

The FFT pipeline is built from a number ( $n$ ) of radix-2 processing stages, giving a complex FFT length of  $2^n$ . Each pipelined stage implements a radix-2 butterfly, twiddle factor application and data re-ordering. Arithmetic overflow is avoided by always applying worst-case scaling.

The input data stream for both types of FFT core consists of normally ordered complex time-domain samples. The HiSpeed core requires In-phase (I) and Quadrature-phase (Q) components to be time interleaved to match the ‘parallelism of 1’ of the core. The QuadSpeed core requires odd and even complex samples to be de-multiplexed to match the parallelism of 4.

The format of the HiSpeed FFT core’s complex frequency-domain data output is time interleaved I and Q. The format of the QuadSpeed FFT core’s complex frequency-domain data output is two parallel complex streams, one covering positive frequencies and the other covering negative frequencies.

All of the library FFTs include an input buffer and bit reverser. The input buffer performs the re-ordering of the input data stream, to the format required for the parallel FFT input. The bit reverser performs efficient reordering of the frequency domain output from the FFT, so that the frequency data is in natural ascending frequency order.

## ***Deliverables***

The FFT library is provided on a single compact disc. All FFT cores are completely stand-alone designs, and include the following items:

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL and VHDL model. Bit-true Matlab model and scripts. Placement reports

### **Deliverables provided for each FFT Core**

A complete list of the supplied FFT cores, including maximum sample rates, power consumption, and silicon usage is provided on the following pages.

## ***Licensing***

The FFT library is provided with a site licence, which permits unlimited use of the core for development and manufacturing purposes at a single customer location or facility.

## FFT Cores for Xilinx Spartan III FPGA

FFT Length (complex)	Architecture	Input bit-width	Output bit-width	Max Clock Rate <sup>1</sup> MHz	Max Sample Rate <sup>2</sup> MS/s	No. Slices	No. RAMs	No. Mults	Power <sup>3</sup> mW
32	HiSpeed	14	18	167.3	83.6	909	4	3	560
64	HiSpeed	14	18	167.7	83.8	1137	5	4	626
128	HiSpeed	14	19	159.3	79.6	1409	6	5	700
256	HiSpeed	14	19	162.5	81.2	1684	7	6	774
512	HiSpeed	14	20	165.2	82.6	2020	9	7	865
1,024	HiSpeed	14	20	167.0	83.5	2454	12	9	1048
2,048	HiSpeed	14	21	154.6	77.3	2801	20	11	1267
4,096	HiSpeed	14	21	153.8	76.6	3111	34	13	1595
8,192	HiSpeed	14	22	123.3	61.6	3422	63	15	1939
32	QuadSpeed	12	16	167.2	334.4	1623	8	9	835
64	QuadSpeed	12	16	155.4	310.8	2047	10	12	966
128	QuadSpeed	12	17	164.9	329.8	2522	10	15	1155
256	QuadSpeed	12	17	142.7	285.4	2952	13	18	1299
512	QuadSpeed	12	18	140.9	281.8	3432	14	21	1499
1,024	QuadSpeed	12	18	127.7	255.4	3907	17	24	1708
2,048	QuadSpeed	12	19	135.0	270.0	4425	22	27	1892
4,096	QuadSpeed	12	19	133.9	267.8	5020	33	30	2125
8,192	QuadSpeed	12	20	131.5	263.0	5672	56	33	2493
16,384	QuadSpeed	12	20	113.4	226.8	8175	99	37	3819

## Notes:

1. The maximum core clock rates quoted above are based on a -5 speed grade device. It should also be noted that the frequencies indicated are placement dependent and as such there may be variations from the stated frequencies when the cores are used.
2. The maximum complex sample rates that can be processed are determined by the clock rate. For the QuadSpeed architecture the maximum complex sample rate is double the clock input, for the HiSpeed architecture it is half the clock input.
3. Power estimates are calculated using the maximum frequency stated and worst-case toggle rates using a suitably sized device.

## FFT Cores for Xilinx Virtex II FPGA

FFT Length (complex)	Architecture	Input bit-width	Output bit-width	Max Clock Rate <sup>1</sup> MHz	Max Sample Rate <sup>2</sup> MS/s	No. Slices	No. RAMs	No. Mults	Power <sup>3</sup> mW
32	HiSpeed	14	18	202.7	101.3	908	4	3	717
64	HiSpeed	14	18	197.8	98.6	1138	5	4	871
128	HiSpeed	14	19	192.8	96.4	1409	6	5	1040
256	HiSpeed	14	19	179.8	89.9	1534	7	6	1159
512	HiSpeed	14	20	184.9	92.4	2020	9	7	1454
1,024	HiSpeed	14	20	183.7	91.8	2453	12	9	1739
2,048	HiSpeed	14	21	165.9	82.9	2801	20	11	2083
4,096	HiSpeed	14	21	173.4	86.7	3112	34	13	2628
8,192	HiSpeed	14	22	170.2	85.1	3428	63	15	3479
16,384	HiSpeed	14	22	135.2	67.6	3765	119	17	4788
32	QuadSpeed	12	16	200.7	401.4	1534	8	9	1178
64	QuadSpeed	12	16	200.8	401.6	2045	10	12	1533
128	QuadSpeed	12	17	200.5	401.0	2522	10	15	1833
256	QuadSpeed	12	17	193.2	386.4	2952	13	18	2151
512	QuadSpeed	12	18	180.4	360.8	3432	14	21	2513
1,024	QuadSpeed	12	18	187.9	375.8	3907	17	24	2934
2,048	QuadSpeed	12	19	187.5	375.0	4423	22	27	3389
4,096	QuadSpeed	12	19	173.6	347.2	5019	33	30	4033
8,192	QuadSpeed	12	20	169.4	338.8	5672	56	33	4825
16,384	QuadSpeed	12	20	153.2	306.4	6470	107	37	6301

## Notes:

1. The maximum sample rates quoted above are based on a -5 speed grade device. It should also be noted that the frequencies indicated are placement dependent and as such there may be variations from the stated frequencies when the cores are used.
2. The maximum complex sample rates that can be processed are determined by the clock rate. For the QuadSpeed architecture the maximum complex sample rate is double the clock input, for the HiSpeed architecture it is half the clock input.
3. Power estimates are calculated using the maximum frequency stated and worst-case toggle rates using a suitably sized device.

## FFT Cores for Xilinx Virtex II Pro FPGA

FFT Length (complex)	Architecture	Input bit-width	Output bit-width	Max Clock Rate <sup>1</sup> MHz	Max Sample Rate <sup>2</sup> MS/s	No. Slices	No. RAMs	No. Mults	Power <sup>3</sup> mW
32	HiSpeed	14	18	229.2	114.6	909	4	3	1124
64	HiSpeed	14	18	227.2	113.6	1138	5	4	1251
128	HiSpeed	14	19	227.4	113.7	1409	6	5	1390
256	HiSpeed	14	19	205.2	102.6	1684	7	6	1532
512	HiSpeed	14	20	204.2	102.1	2020	9	7	1708
1,024	HiSpeed	14	20	202.3	101.1	2453	12	9	1945
2,048	HiSpeed	14	21	200.0	100.0	2801	20	11	2318
4,096	HiSpeed	14	21	203.4	101.7	3107	34	13	2861
8,192	HiSpeed	14	22	200.3	100.1	3422	63	15	3483
16,384	HiSpeed	14	22	194.4	97.2	3759	119	17	4698
32,768	HiSpeed	14	23	155.2	77.6	4145	234	19	6893
32	QuadSpeed	12	16	251.9	503.8	1623	8	9	1607
64	QuadSpeed	12	16	250.1	500.2	2047	10	12	1853
128	QuadSpeed	12	17	250.1	500.2	2523	10	15	2096
256	QuadSpeed	12	17	251.7	503.4	2952	13	18	2361
512	QuadSpeed	12	18	250.4	500.8	3432	14	21	2624
1,024	QuadSpeed	12	18	249.8	499.6	3907	17	24	2905
2,048	QuadSpeed	12	19	214.4	428.8	4424	22	27	3420
4,096	QuadSpeed	12	19	199.4	398.8	5019	33	30	3862
8,192	QuadSpeed	12	20	205.9	411.8	5673	56	33	4710
16,384	QuadSpeed	12	20	197.2	394.4	6470	107	37	5895
32,768	QuadSpeed	12	21	160.2	320.4	7398	209	41	8126

## Notes:

1. The maximum sample rates quoted above are based on a -6 speed grade device. It should also be noted that the frequencies indicated are placement dependent and as such there may be variations from the stated frequencies when the cores are used.
2. The maximum complex sample rates that can be processed are determined by the clock rate. For the QuadSpeed architecture the maximum complex sample rate is double the clock input, for the HiSpeed architecture it is half the clock input.
3. Power estimates are calculated using the maximum frequency stated and worst-case toggle rates using a suitably sized device.

## Associated Products and Services

### FFT Ancillary Cores

RF Engines provide a full range of signal processing cores that can be quickly and easily integrated with the Library FFT cores in order to produce complete spectral analysis systems. These cores, not supplied with the FFT Library, can be provided as standalone items, or RF Engines can provide integration services to produce a complete system on FPGA. Ancillary cores include:

**Distributed Half-Band Filters** These cores can be used to efficiently convert a real stream of samples to a complex format at half the sample rate. This enables efficient use of the complex FFTs for processing real data.

**Window Function** In most FFT systems it is desirable to weight the incoming samples in order to improve the frequency response of each FFT bin. RF Engines have efficient windowing solutions available that include both fixed and reprogrammable window coefficients.

**Power Block Accumulator** RF Engines' power block can be used to convert the output of an FFT to a power spectrum, and then accumulate successive FFT blocks. This technique is often used to produce an average power spectrum, thereby reducing the output data rate from the FPGA.

**CORDIC** The CORDIC (Coordinate Rotation Digital Computer) can be used at the output of the FFT to convert the complex samples to amplitude and phase values.

### Custom FFT Designs

Whilst the FFT cores provided with FFT Library meet the majority of requirements for high-speed spectral analysis, there are occasions where a custom design is required. RF Engines have a variety of existing architectures that can generally be customised to meet most FFT requirements within very short timescales. Example customisations include:

- Tailoring FFT bit widths to meet specific dynamic range and silicon usage requirements
- Real input FFTs
- Multiplexing several channels through a single FFT core
- Selectable length FFT transforms
- Multi-resolution FFTs (efficiently performing multiple transform lengths simultaneously)
- 2-Dimensional FFTs

RF Engines can also provide FFT cores for Altera and other leading FPGAs.

### HyperSpeed and HyperLength FFTs

The **HyperSpeed** FFT range is designed for use in applications where very high sample rates are required, and achieves rates of up to 6.4GS/s complex.

The **HyperLength** FFT is designed to implement very long transforms with minimum memory bandwidth. When used in conjunction with SRAM memory the architecture will support a 1M-point transform running at complex sample rates up to 200MS/s. The use of SDRAM, will allow transform lengths up to 256M-points, at rates up to 10MS/s.

For more information on these and other products and services from RF Engines, please consult our website at [www.rfel.com](http://www.rfel.com), or email us at [info@rfel.com](mailto:info@rfel.com).



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