



## OVERVIEW

This document describes RFEL's Numerically Controlled Oscillator (NCO) core. This core provides interleaved complex sinusoidal outputs in continuous real time, with no gaps in the data, at complex data rates of up to 100MS/s. An alternative variant of the core provides real or complex sinusoidal output at data rates of up to 200MS/s.

Numerically controlled oscillators are a silicon efficient means of generating sinusoidal signals with very low quantisation spurs. They are useful in situations where a continuous phase sinusoidal signal with variable frequency is required. An NCO can be combined with a complex multiplier to provide a frequency shift to an existing complex signal, for instance in correcting frequency offset in a communications signal.

RFEL's NCO core is intended for use in applications where processing speed is critical and optimum use of available silicon is required. The core is available for licence in netlist form as a component ready to be combined with customer's own IP.

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## FEATURES

- Continuous interleaved complex sinusoidal data at up to 100MS/s
  - Continuous real or complex sinusoidal outputs at up to 200MS/s
  - Fully pipelined design
  - Targeted at Xilinx and Altera FPGA families
  - Bit-widths adjustable at factory
  - Fully bit-true parameterisable models are available
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## APPLICATIONS

- Frequency shifting in variable filter banks
- Correction of frequency offset in communications systems
- Electronic warfare (radar, sonar, surveillance)
- Medical instrumentation
- Test instrumentation
- Real-time spectral analysis

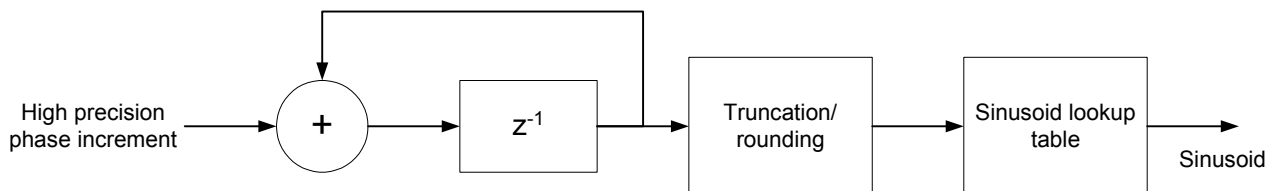
The NCO is most often used to provide fine frequency calibration for wideband signals.

## GENERAL DESCRIPTION

The concept behind the NCO core is as shown in Figure 1. A high precision input phase increment is accumulated over time to provide a very accurate time-varying phase location for a sinusoid at a particular frequency. This phase location is then truncated and used to address a sinusoid lookup table with far fewer address locations. The output of this lookup table is a sinusoid with frequency defined by the input phase increment. The relationship between the input phase increment and the sinusoid frequency is given by:

$$p = \text{round}(2^W \cdot f / f_s)$$

where  $f$  is the required sinusoid frequency,  $f_s$  is the data rate,  $W$  is the accumulator width and  $p$  is the required phase increment.



**Figure 1: NCO decomposition**

The NCO described can be relatively simply modified to produce complex interleaved sinusoidal output data. Such an NCO can be combined with a complex multiplier at the output to apply variable frequency shifts to a complex input signal.

A particular variant of the NCO core was designed by RFEL to correct frequency offset in a much larger communications core. The real ADC output at 200MS/s was first passed through RFEL's DHBF fixed downconverter core to provide a 100MS/s complex interleaved signal centred around DC. A known time-varying frequency offset was then corrected by multiplying the complex DHBF output with the output of an NCO core. The core parameters are shown in Table 1; the pipelined interleaved complex multiplier is included as part of this variant of the NCO core.

Parameter	Value
Data input width	14
Data output width	14
Accumulator width	27
LUT width	17
LUT address width	14
Max data rate	202MHz
Device	Xilinx Virtex-II Pro 50 -5
Slices	262
Multipliers	4
RAMs	5

**Table 1: Example core parameters**



### CORE INTERFACE DESCRIPTION

Signal	Direction	Type	Width	Function
clk	IN	std logic	1 bit	The core clock rate for the interleaved complex core is equal to $f_s$ where $f_s=2f_{in}$ and $f_{in}$ is the input sample rate.
reset_in	IN	std logic	1 bit	Active-high pulse that resets the phase accumulator.
enable_in	IN	std logic	1 bit	Active-high signal asserted for the block to keep processing. Asserted from first sample of input data.
data_in	IN	std logic vector	(data_width_in -1 downto 0)	2's complement data input.
data_out	OUT	std logic vector	(data_width_out -1 downto 0)	2's complement data output.

**Table 2: Interface specification**

### DELIVERABLES

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL VHDL Model. Bit-true Matlab model and scripts. Placement reports.

**Table 3: Items provided with each core**

Electronic transfer is used to deliver the cores and supporting documentation.

Optional design support services are available to help incorporate the core into larger designs.

**GLOSSARY**

<b>ADC</b>	Analogue to Digital Converter
<b>EDIF</b>	Electronic Data Interchange Format
<b>FPGA</b>	Field Programmable Gate Array
<b>I/O</b>	Input / Output
<b>MS/s</b>	Million Samples Per Second
<b>NCO</b>	Numerically Controller Oscillator
<b>RFEL</b>	RF Engines Limited
<b>RTL</b>	Register Transfer Level
<b>UCF</b>	User Constraints File
<b>VHDL</b>	Very High Speed IC Hardware Description Language
<b>VITAL</b>	VHDL Initiative Toward ASIC Libraries

**Table 4: Glossary**

Please refer to the RFEL web site [www.rfel.com](http://www.rfel.com) for details of other signal processing IP cores.

Specifications are subject to change without notice.