



OVERVIEW

This document describes a specific variant in RFEL's Matrix 'Dual-Speed' range of Mixed-Radix FFT cores. This specific core processes complex input data in continuous real time, with no gaps in the data, at complex data rates of up to 200 MS/s.

For many applications the radix-2 FFT [1][2] provides an adequate solution; however, there are some applications where a non-power-of-two number of FFT points is required - for instance to provide a particular frequency bin spacing at the output which is not a power-of-two division of the input frequency span. RFEL have 2-point [3], 3-point [4] and 13-point [5] DFT cores available that may be combined to form a large number of possible FFT sizes. Further DFT designs are available, including 4, 5, 7, 8 and 11-point DFTs; though these have not yet been implemented in silicon.

The example core described here implements a 1872-point DFT using a mixed radix FFT composed of 4x2-point DFTs, 2x3-point DFTs and a single 13-point DFT. This core was part of a larger channeliser core and permitted an exact channel spacing to be achieved with the exact required output sample rate.

RFEL's Matrix DFT/FFT cores are intended for use in applications where processing speed is critical and optimum use of available silicon is required. The core is available for licence in netlist form as a component ready to be combined with customer's own IP. Alternatively RFEL can provide the core in bitstream format for a complete chip design.

FEATURES

- Continuous real time processing of complex data at up to 200MS/s
- Compatible with 400MS/s ADC using RFEL's optional DHBF core
- Fully pipelined design
- Targeted at Xilinx and Altera FPGA families
- Bit-widths and bit-growths adjustable at factory
- Fully bit-true parameterisable models are available
- Other DFT sizes available

APPLICATIONS

- Wide-band filter banks.
- Communications systems with exact required bin spacing.
- Electronic warfare (radar, sonar, surveillance)
- Medical instrumentation
- Test instrumentation
- Real-time spectral analysis

GENERAL DESCRIPTION

The 1872-point FFT core takes blocks of 1872 time domain samples in complex I and Q format and efficiently calculates the 1872-point DFT to obtain a block of 1872 complex frequency domain samples.

The core uses a mixed radix FFT architecture with the following radices: 2, 2, 2, 2, 3, 3, 13. The architecture is shown in Figure 1. The 3 and 13-point DFTs are implemented using the Winograd Fast Transform Algorithm (WFTA) in a serial architecture (see [4][5]). An input buffer is required at the front-end to rearrange the samples to the correct order for the radix-2 input stage, reorder blocks are used between stages, and a reorder block is included at the output. The output reorder block is analogous to a bit-reverser in a radix-2 FFT design.

Twiddle blocks are also supplied where necessary but, to reduce the number of multipliers, the twiddleless FFT technique was used to eliminate the twiddle multiplication at the boundary between the radix-2 and radix-3 stages and the boundary between the radix-3 and radix-13 stages. This was significant for the example design since it was being incorporated into a larger channeliser design and the requirement was to minimise the multiplier usage.

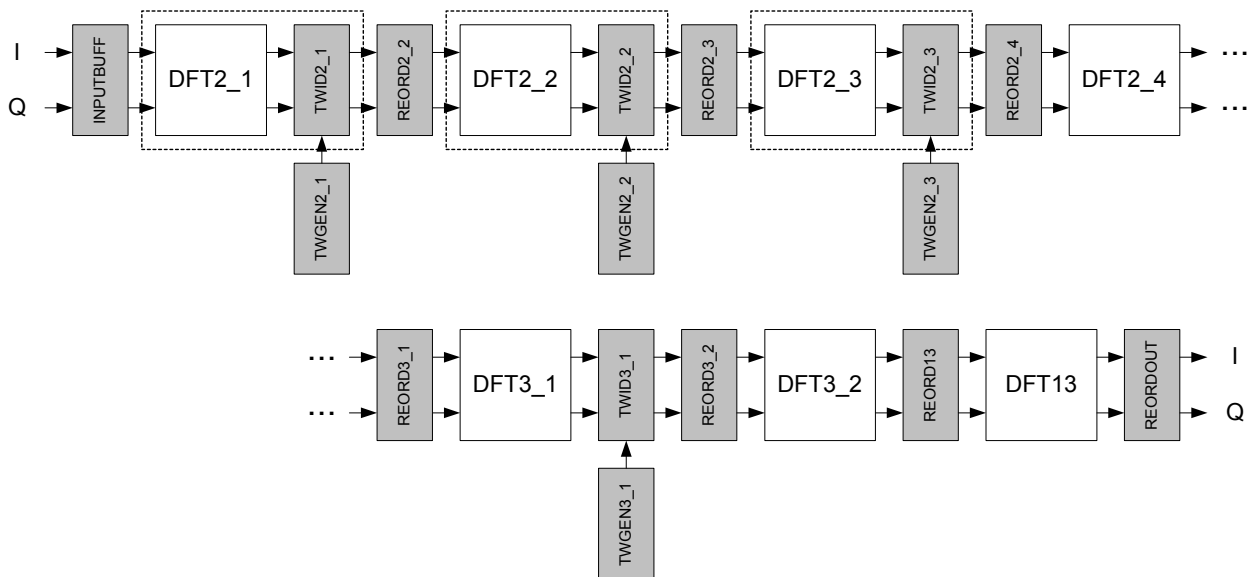


Figure 1: Mixed-Radix FFT Structure

The parameters for the specific variant of the core described here are shown in Table 1.



Parameter	Value
Input width	16
Output width	18
Twiddle width	18
Max clock rate	195MHz
Max data rate	195MHz
Device	Xilinx Virtex-II Pro 50 -5
Slices	9506
Multipliers	28
RAMs	42

Table 1: Example core parameters**CORE INTERFACE DESCRIPTION**

Signal	Direction	Type	Width	Function
clk	IN	std logic	1 bit	The core clock rate is equal to f_s where f_s is the complex input rate.
sync_in	IN	std logic	1 bit	Active-high pulse marking the first sample of a new input block.
enable_in	IN	std logic	1 bit	Active-high signal asserted for a duration equal to the FFT block length. Asserted one clock period before the first sample of complex input data.
data_in_i	IN	std logic vector	(data_width_in -1 downto 0)	2's complement in-phase time-domain data input.
data_in_q	IN	std logic vector	(data_width_in -1 downto 0)	2's complement quad-phase time-domain data input.
sync_out	OUT	std logic	1 bit	Active-high pulse marking the first transformed sample of a new output block. Coincident with the first transformed sample of a new output block.
enable_out	OUT	std logic	1 bit	Active-high signal asserted for 2 samples. Asserted one clock period after the first transformed sample of a new output block.
data_out_i	OUT	std logic vector	(data_width_out -1 downto 0)	2's complement in-phase frequency-domain data.
data_out_q	OUT	std logic vector	(data_width_out -1 downto 0)	2's complement quad-phase frequency-domain data.

Table 2: Interface specification



DELIVERABLES

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL VHDL Model. Bit-true Matlab model and scripts. Placement reports.

Table 3: Items provided with each core

Electronic transfer is used to deliver the cores and supporting documentation.

Optional design support services are available to help incorporate the core into larger designs.

GLOSSARY

ADC	Analogue to Digital Converter
DFT	Discrete Fourier Transform
DHBF	Distributed Half-Band Filter
EDIF	Electronic Data Interchange Format
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
I/O	Input / Output
MS/s	Million Samples Per Second
RFEL	RF Engines Limited
RTL	Register Transfer Level
UCF	User Constraints File
VHDL	Very High Speed IC Hardware Description Language
VITAL	VHDL Initiative Toward ASIC Libraries

Table 4: Glossary

Please refer to the RFEL web site www.rfel.com for details of PFFT cores under development.

Specifications are subject to change without notice.



REFERENCES

- [1] 'Hi-Speed' Product Specification, RF Engines, 12/11/2003.
- [2] 'Quad-Speed' Product Specification, RF Engines, 23/02/2004.
- [3] 2-point 'Dual-Speed' DFT Product Specification, RF Engines, 27/04/2004.
- [4] 3-point 'Dual-Speed' DFT Product Specification, RF Engines, 27/04/2004.
- [5] 13-point 'Dual-Speed' DFT Product Specification, RF Engines, 27/04/2004.