



## OVERVIEW

This document describes the RFEL 2-point 'Dual-Speed' DFT core, which belongs to RFEL's Matrix range. The core processes complex input data in continuous real time, with no gaps in the data, at complex data rates of up to 200 MS/s.

For many applications the radix-2 FFT [1][2] provides an adequate solution; however, there are some applications where a non-power-of-two number of FFT points is required - for instance to provide a particular frequency bin spacing at the output which is not a power-of-two division of the input frequency span. This core may be combined with RFEL's other Matrix DFT cores for problems that require such a mixed-radix solution (see for example [3]).

The core is intended for use in applications where processing speed is critical and optimum use of available silicon is required. The core is available for licence in netlist form as a component ready to be combined with customer's own IP. Alternatively RFEL can provide the 2-point DFT as part of a larger mixed-radix core in either netlist or bitstream format.

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## FEATURES

- Continuous real time processing of complex data at up to 200MS/s
  - Compatible with 400MS/s ADC using RFEL's optional DHBF core
  - Fully pipelined design
  - Targeted at Xilinx and Altera FPGA families
  - Bit-widths and bit-growths adjustable at factory
  - Fully bit-true parameterisable models are available
  - Other DFT sizes available
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## APPLICATIONS

- Wide-band filter banks.
- Communications systems with exact required bin spacing.
- Electronic warfare (radar, sonar, surveillance)
- Medical instrumentation
- Test instrumentation
- Real-time spectral analysis

This core is most likely to be useful as part of an FFT where an exact bin spacing/sample rate combination is required at the FFT output.



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**GENERAL DESCRIPTION**

The 2-point DFT can be used to implement a radix-2 stage in a DIF FFT. It takes pairs of time domain samples in complex I and Q format and uses a serial architecture to calculate the 2-point DFT, providing a pair of complex frequency domain samples. It also optionally provides a complex multiply on the lower output branch to permit twiddling of the output in building the larger FFT.

One version of the core was combined with 3-point and 13-point DFT [4][5] cores to provide an 1872-point FFT [1] as part of a larger channeliser core. This DFT permitted an exact channel spacing to be achieved with an exact output sample rate. The 2-point DFT core parameters are given in Table 1.

<b>Parameter</b>	<b>Value</b>
Input width	16
Output width	17
Twiddle width	18
Max clock rate	200MHz
Max data rate	200MHz
Device	Xilinx Virtex-II Pro 50 -5
Slices	263
Multipliers	2
RAMs	0

**Table 1: Example core parameters**

**CORE INTERFACE DESCRIPTION**

Signal	Direction	Type	Width	Function
clk	IN	std logic	1 bit	The core clock rate is equal to $f_s$ where $f_s$ is the complex input rate.
sync_in	IN	std logic	1 bit	Active-high pulse marking the first sample of a new input block.
enable_in	IN	std logic	1 bit	Active-high signal asserted for a duration equal to the FFT block length. Asserted one clock period before the first sample of complex input data.
data_in_i	IN	std logic vector	(data_width_in -1 downto 0)	2's complement in-phase time-domain data input.
data_in_q	IN	std logic vector	(data_width_in -1 downto 0)	2's complement quad-phase time-domain data input.
sync_out	OUT	std logic	1 bit	Active-high pulse marking the first transformed sample of a new output block. Coincident with the first transformed sample of a new output block.
enable_out	OUT	std logic	1 bit	Active-high signal asserted for 2 samples. Asserted one clock period after the first transformed sample of a new output block.
data_out_i	OUT	std logic vector	(data_width_out -1 downto 0)	2's complement in-phase frequency-domain data.
data_out_q	OUT	std logic vector	(data_width_out -1 downto 0)	2's complement quad-phase frequency-domain data.

**Table 2: Interface specification****DELIVERABLES**

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL VHDL Model. Bit-true Matlab model and scripts. Placement reports.

**Table 3: Items provided with each core**

Electronic transfer is used to deliver the cores and supporting documentation.

Optional design support services are available to help incorporate the core into larger designs.

**GLOSSARY**

<b>ADC</b>	Analogue to Digital Converter
<b>DFT</b>	Discrete Fourier Transform
<b>DHBF</b>	Distributed Half-Band Filter
<b>EDIF</b>	Electronic Data Interchange Format
<b>FFT</b>	Fast Fourier Transform
<b>FPGA</b>	Field Programmable Gate Array
<b>I/O</b>	Input / Output
<b>MS/s</b>	Million Samples Per Second
<b>RFEL</b>	RF Engines Limited
<b>RTL</b>	Register Transfer Level
<b>UCF</b>	User Constraints File
<b>VHDL</b>	Very High Speed IC Hardware Description Language
<b>VITAL</b>	VHDL Initiative Toward ASIC Libraries

**Table 4: Glossary**

Please refer to the RFEL web site [www.rfel.com](http://www.rfel.com) for details of PFFT cores under development.

Specifications are subject to change without notice.

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**REFERENCES**

- [1] 'Hi-Speed' Product Specification, RF Engines, 12/11/2003.
- [2] 'Quad-Speed' Product Specification, RF Engines, 23/02/2004.
- [3] Mixed-Radix 'Dual-Speed' FFT Product Specification, RF Engines, 27/04/2004.
- [4] 3-point 'Dual-Speed' DFT Product Specification, RF Engines, 27/04/2004.
- [5] 13-point 'Dual-Speed' DFT Product Specification, RF Engines, 27/04/2004.