



OVERVIEW

This document describes the RFEL Vectis 'HiSpeed' range of Pipelined FFT (PFFT) cores. The cores process complex input data in continuous real time, with no gaps in the data, at complex data rates in excess of 100 MS/s. This document provides details of the cores and design services available from RFEL.

Vectis HiSpeed cores are intended for use in applications where processing speed is critical and optimum use of available silicon is required. The cores are available for licence in netlist form as a component ready to be combined with customer's own IP. Alternatively, where the core is to be the *only* contents of an FPGA, it can be provided as a programming bitstream; in this case RFEL would provide a separate design services contract.

FEATURES

- Continuous real time processing of complex data in excess of 100MS/s
 - Compatible with 200MS/s ADC using RFEL's optional DHBF core
 - Fully pipelined design
 - Targeted at Xilinx and Altera FPGA families
 - 8 to 128K-point versions available (longer lengths by request)
 - Bit-width and bit-growth adjustable at factory
 - Twiddle bit-width adjustable at factory
 - Internal memory partitioning adjustable at factory
 - Can be used for real-input FFTs with additional modules
 - Fully bit-true parameterisable models are available
 - Optional input buffer and bit reverser
 - FFT and IFFT functionality
 - 2xOversampled option.
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APPLICATIONS

- Wide-band filter banks
 - Communications systems
 - Electronic warfare (radar, sonar, surveillance)
 - Medical instrumentation
 - Test instrumentation
 - Real-time spectral analysis
 - Multi-channel systems, where many low speed channels are interleaved through the high-speed core.
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GENERAL DESCRIPTION

The Vectis HiSpeed range is based on a radix-2 Decimation-in-Frequency (DIF) pipelined FFT. The architecture is based on 'n' successive stages, where 2^n is the size of the FFT. Each stage has switched delay elements and butterflies. The switches and delays of each stage re-order the data into the correct order for processing by the butterfly. There are 'n' butterflies, each performing a 2-point Discrete Fourier Transform (DFT) and complex phase rotations (twiddles). Figure 1 below shows the basic architecture of the cores.

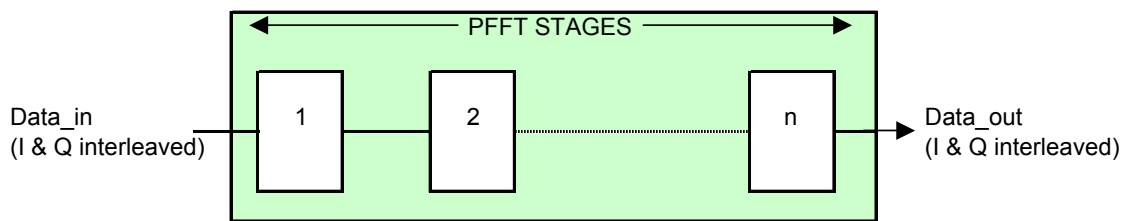


Figure 1: Vectis HiSpeed n-point PFFT

EXAMPLES USED IN THIS DOCUMENT

To limit the diagrams to a convenient size, a 16-point PFFT is used in the examples below.

FFT INPUT FORMATS

FFT with Input Buffer

The PFFT core can be supplied with an optional Input Buffer that formats the data as required for the PFFT function. The format of the PFFT data input is signed 2's-complement. With the Input Buffer included the I and Q data samples must be interleaved as shown in Figure 2 below.

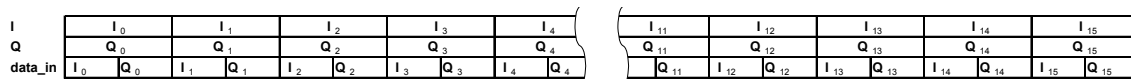


Figure 2: 16-point PFFT Data Input Format Example with Input Buffer Included

'I' and 'Q' show the original 16 naturally time-ordered complex data samples at a complex sample frequency, f_s , before interleaving. 'data_in' shows these samples interleaved as required for input to the core.

Note the input data rate into the core after interleaving is $2f_s$. The PFFT core must be clocked at this rate of $2f_s$.

If a 2xoversampled PFFT core is supplied a clock rate of $4f_s$ is required, with 'data_in' interleaved as shown at a rate of $2f_s$.

FFT without Input Buffer

If the PFFT core is supplied with no Input Buffer option selected then the input data must be interleaved, as shown in Figure 3.

For a 2xoversampled PFFT core an Input Buffer option is selected as standard.

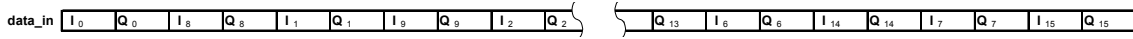


Figure 3: 16-point PFFT Data Input Format Example with No Input Buffer Included

FFT OUTPUT FORMATS

FFT with Bit Reverser

The format of the PFFT core data output is signed 2's-complement at the PFFT core clock rate. This format can be converted to other formats by the addition of separate modules available from RFEL. The PFFT core can be supplied with an optional Bit Reverser that reorders the complex frequency samples to be in the time orders as shown in Figure 4 and Figure 5 below, depending on the state of the '*natural_freq_order*' core input.

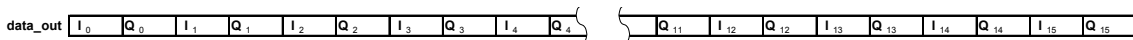


Figure 4: 16-point PFFT Data Output with Bit Reverser and No Frequency Shifting

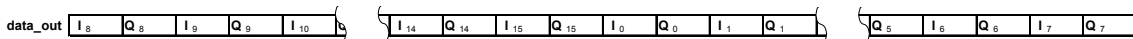


Figure 5: 16-point PFFT Data Output with Bit Reverser and Frequency Shifting

FFT without Bit Reverser

If the PFFT core with no Bit Reverser option is selected then the output complex frequency samples are in a bit-reversed time order as shown in Figure 6 and Figure 7 below, depending on the state of the '*natural_freq_order*' core input.

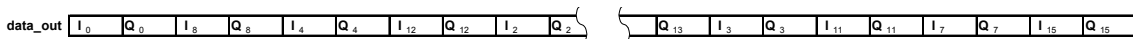


Figure 6: 16-point PFFT Data Output with No Bit Reverser and No Frequency Shifting

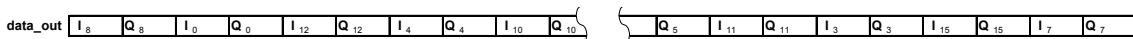


Figure 7: 16-point PFFT Data Output with No Bit Reverser and Frequency Shifting

Frequency Sample Output Centre Frequency

For the 16 sample PFFT example, the centre frequency of each complex frequency sample is given by the following equation:-

$$\text{Bin Frequency}(n) = n * f_s / 16$$

Where n is the complex output frequency sample number in the range 0 to 15, and f_s is the original complex sample frequency as shown by I and Q of Figure 2.

Or in general terms, $Bin\ Frequency(n) = n * f_s / FFT_size$

Frequency Shifted Output

The output sequence of the PFFT core can be provided with an $N/2$ frequency shift, where N is the FFT length. This is controlled using the core input '*natural_freq_order*' and allows the output sample sequence to start with either: -

- Nyquist centre bin, ($n=0$), when '*natural_freq_order*' is logic '0'
- Nyquist start bin, ($n = N/2$), when '*natural_freq_order*' is logic '1'

Figure 4 / Figure 6 above illustrates the natural frequency sample output order when '*natural_freq_order*' is logic '0'. Figure 5 / Figure 7 illustrates the shifted frequency sample output order when '*natural_freq_order*' is logic '1'.

It is important to note that the '*natural_freq_order*' signal is intended to be a 'static' input. If '*natural_freq_order*' is changed while the PFFT core is processing data, then the current block of data will not be output correctly.

CORE INPUT SYNCHRONISATION

The PFFT can process input data blocks continuously (back to back with no gaps in time) or as discrete time separated blocks. In either case, the core requires the active high '*sync_in*' signal to be active for one clock period, two clock periods prior to the first complex sample. It also requires the active high '*enable_in*' signal to be asserted for a duration equal to the PFFT block size; one clock period prior to the first complex sample, as shown in the 16-point timing diagram example of Figure 8 below.

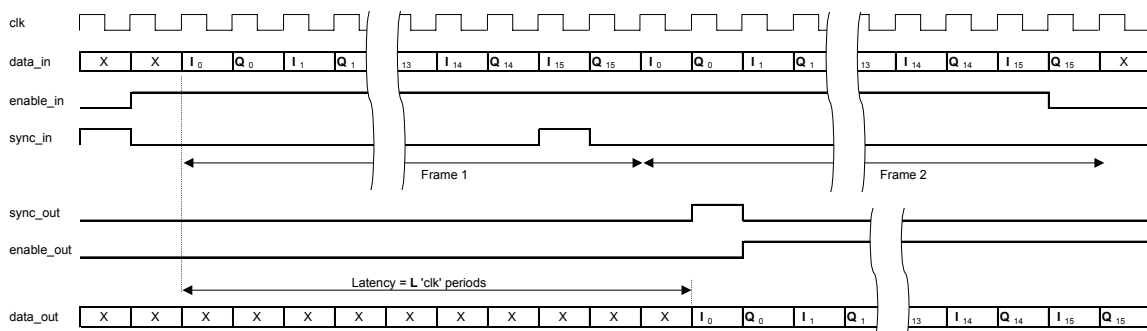


Figure 8: 16-point PFFT I/O Timing Diagram Example

CORE OUTPUT SYNCHRONISATION

The first complex sample of each output block is marked by the active-high '*sync_out*'. The active high '*enable_out*' signal is also asserted for a duration equal to the PFFT block size; one clock period after the first complex sample as shown in the timing diagram example of Figure 8 above.

Figure 8 above is illustrated showing a PFFT core combination with Input Buffer present, Bit Reverser present and no frequency shifting using the '*natural_freq_order*' signal input. The relative timing of input control and data and output control and data signals is the same for all combinations of PFFT core with or without Input Buffer and Bit Reverser. The latency however is different for each of these options, as described later.

IFFT OUTPUT

The PFFT core is also able to produce an IFFT computation. This is controlled using the core input '*fft_ifft*' and allows the output sample sequence to be either: -

- FFT of input complex samples when '*fft_ifft*' is logic '1'
- IFFT of input complex samples when '*fft_ifft*' is logic '0'

It is important to note that the '*fft_ifft*' signal is intended to be a 'static' input. If '*fft_ifft*' is changed while the PFFT core is processing data, then several blocks of data will be output incorrectly. The number of 'corrupt' blocks will be dependent on the pipeline latency of the PFFT core.



LATENCY

Latency, defined as the time from when the first complex sample of an input block is clocked into the PFFT to the time when the first transformed complex frequency output sample is clocked out from the PFFT, is shown in the timing diagram example of Figure 8 above.

The latency can be calculated by:

$$'L' = t_{ib} + t_{fft} + t_{sp} + t_{wm} + t_{br} \text{ PFFT core clock periods.}$$

Where

$$t_{ib} = \text{input_buffer_present} \times (N - 1) \text{ or } (2N - 1) \text{ if 2xoversampled core option}$$

$$t_{fft} = 2N + 19 \times \log_2(N) - 30$$

$$t_{sp} = 3 \times \text{speed_option_selected} \times (\log_2(N) - 2)$$

$$t_{wm} = \text{sum}(\min(1, \max(0, \text{stage_widths}(2:\text{end}-3)-17)))$$

$$t_{br} = (2N - 2^{\lfloor (\log_2(N) + 1) / 2 \rfloor} - 2^{\lfloor (\log_2(N) + 2) / 2 \rfloor} + 9) \times \text{bit_reverser_present}$$

'N' is the FFT length.

'input_buffer_present', when PFFT core has the Input Buffer function included assign a value of 1 to include it's latency else assign a value of 0.

'speed_option_selected', when true, adds some pipelining to increase the performance of the core. This option is a factory-selected option that depends on the maximum sample rate required (increases the clock rate by approx 10% if required). Assign a value of 1 to include its latency else assign a value of 0.

'stage_widths' is an array of butterfly stage input bit widths. Additional pipelining is required when the butterfly multiplications exceed 18-bits.

'bit_reverser_present', when PFFT core has the Bit Reverser function included assign a value of 1 to include it's latency else assign a value of 0.

For the 16 sample PFFT example, assuming a combination of input buffer present, bit reverser present, speed option not selected and no stage widths exceeding 18-bit multiplications: -

$$'L' = (16-1) + (2 \times 16 + 19 \times 4 - 30) + 0 + 0 + (2 \times 16 - 4 - 8 + 9)$$

$$'L' = 149 \text{ PFFT core clocks.}$$

The PFFT core is a continuous pipeline so after the initial delay due to the pipeline filling up, as described previously, valid data is continuously available at the output.

CORE INTERFACE DESCRIPTION

All core inputs should be synchronised to the 'clk' signal. All core outputs are synchronised by the 'clk' signal.

Signal	Direction	Type	Width	Function
clk	IN	Std logic	1 bit	The core clock rate is equal to $2f_s$ or $4f_s$ for the 2xoversampled option. Where f_s is the complex input rate.
rst_p	IN	Std logic	1 bit	An active-high pulse, of duration greater than 2 core clock periods, resets the PFFT control logic, but not the PFFT pipeline.
sync_in	IN	Std logic	1 bit	Active-high pulse marking the first sample of a new input block. Precedes first sample of complex input data by two clock periods.
enable_in	IN	Std logic	1 bit	Active-high signal asserted for a duration equal to the PFFT block length. Asserted one clock period before the first sample of complex input data.
natural_freq_order	IN	Std logic	1 bit	If logic '0' Nyquist centre bin is output first, else Nyquist start bin is output first. (Performs an 'fftshift' function).
fft_ifft	IN	Std logic	1 bit	Active-high signal to select FFT function, else an IFFT function is performed.
data_in	IN	Std logic vector	(data_width_in - 1 downto 0)	2's complement interleaved time-domain data
sync_out	OUT	Std logic	1 bit	Active-high pulse marking the first transformed sample of a new output block. Coincident with the first transformed sample of a new output block.
enable_out	OUT	Std logic	1 bit	Active-high signal asserted for a duration equal to the PFFT block length. Asserted one clock period after the first transformed sample of a new output block.
data_out	OUT	Std logic vector	(data_width_out - 1 downto 0)	2's complement interleaved frequency-domain data.

Table 1: PFFT Interface Specification

N.B. A reduction in core power can be obtained by inhibiting the 'sync_in' signal. This power-save mode can be used whenever the core is not required to operate in continuous mode.

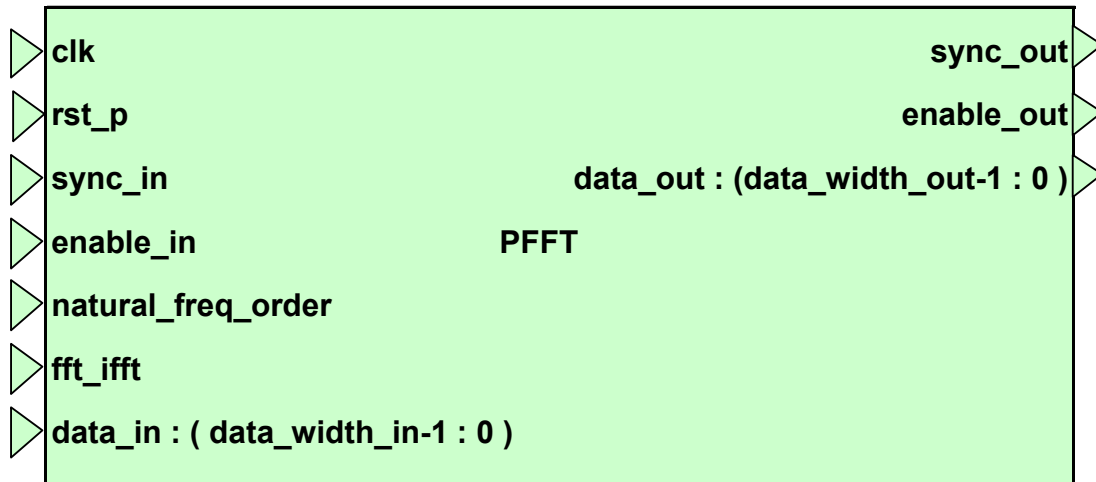


Figure 9: PFFT Symbol

POWER REQUIREMENTS

The power requirement for any particular core will be highly dependent on the target device, size of implementation, and clock rate. RFEL can provide individual power estimates for a particular design if required. See Case Studies for some examples.

VERIFICATION

Verification of the core is achieved in several distinct phases in the design cycle.

Initially, a bit-true Matlab model of the core is used to provide reference output data, using a specific set of input stimuli. These models exactly match the behaviour of the hardware architecture and their outputs are bit-true representations of the actual core.

The input stimuli are used to functionally (pre-synthesis) test the VHDL code using the ModelSim simulator. The results of these simulations are automatically compared with the reference data generated by the bit-true Matlab model and pass/fail indications are reported.

After the VHDL has been synthesised and place-and-route of the core is complete, timing simulations, based on the chip vendor's simulation netlist and gate delay files for the core are performed. These also take the form of the functional tests, but being based on the compiled netlist and timing files from the FPGA vendor, they verify the expected timings of the delivered core.

The bit-true Matlab models are also included.



DELIVERABLES

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL VHDL Model. Bit-true Matlab model and scripts. Placement reports.

Table 2: Items provided with each core

Electronic transfer is used to deliver the cores and supporting documentation.
Optional design support services are available to help you incorporate the core into your design.

INFORMATION REQUIRED FOR QUOTATION

To enable RFEL to provide the required PFFT core, select from the options list below the required parameters and contact us at 'sales@rfel.com'

- Product** = Vectis 'HiSpeed' or Vectis 'QuadSpeed'
- Radix* = Currently only Radix 2 available as off the shelf
- Length* = (powers of 2 from 8 through 131072)
- Target technology*
 - 'XV2P' = Xilinx Virtex-II PRO
 - 'AS' = Altera Stratix
 - 'XV2' = Xilinx Virtex-II
 - 'SP3' = Xilinx Spartan3
- Speed grade* = technology specific '6 for example'
- Input bit-width* = 8 to 22 bits
- Twiddle bit-width* = 10 to 18 bits
- Output bit-width* = 8 to 32 bits
- Precision*
 - H = High Precision (1 bit growth per stage).
 - S = Single Multiplier (17 bits used at each stage),
 - U = user definable (defined prior to order).
- IB* = Input buffer included in core
- IB2X* = 2 x over-sampled Input buffer included in core
- BR* = Bit-reverser included in core.

* Data sheet is for HiSpeed product only.

In addition f_s , Max Complex Input Sample Rate will need to be specified.

For examples of the product part number required for order refer to the Case Studies section.



ARITHMETIC PRECISION OPTIONS

The arithmetic precision used within an FFT core will determine the accuracy of the results. The Vectis range of Pipelined FFT cores allows the arithmetic precision of each butterfly stage to be specified to provide an optimal solution in terms of silicon and performance.

The three precision options offered are described below:-

H (High Precision) Growing the arithmetic precision by one bit per radix-2 stage is generally more than most systems require, but it provides the best spurious free performance, system noise level and magnitude and phase accuracies. Obviously this option will lead to a larger implementation compared with one that is tightly tailored to the performance requirements of the system. In many cases, the hardware overhead is not significant (see Case Study 'Virtex II PRO and Spartan3 Placed and Routed Device Utilisation and Maximum Clock Rate).

S (Single Multiplier Precision) The Virtex-II / PRO, Spartan3 and Altera Stratix architectures contain 18-bit x 18-bit signed multiplier blocks. This precision option ensures that only one of these multiplier blocks is required for each butterfly stage rather than the two blocks that would be required for stage bit widths of 18-bits and over. The result is a core that is optimal in terms of logic and multiplier resource, but has a limited spurious free performance and magnitude and phase accuracy.

U (User-Defined Precision) This option allows the core to be optimised to meet the user's system performance requirements with the minimum of silicon.

RFEL has extensive experience and a range of analysis tools that allow us to assess bit-true system performance. Parameters such as spurious free dynamic range, system noise characteristics, magnitude and phase accuracy, etc. can be measured for various arithmetic precisions, to allow an optimal solution to be developed.

RFEL offer parameterisable bit-true models that match the behaviour of our cores exactly. These models allow system engineers to investigate the precision trade-offs within their own system before ordering.

The maximum input range of the 'HiSpeed cores' is determined by input bit width and is given using the formula $(2^{(\text{input_bit_width} - 1)} - 1)$.

ENGINEERING SUPPORT SERVICES AND MODELS

Accuracy and precision are system design considerations that affect data and twiddle bit-widths. RFEL can offer system-engineering advice to aid the selection of the optimal core configuration.

RFEL also offer system-engineering advice to assist in the selection of an optimal core for the system requirement. For example accuracy, precision and spurious free dynamic range/noise floor can all be modelled using Matlab bit-true models. This ensures input and output bit-widths, twiddle bit-width and arithmetic bit growth at each stage can all be optimised, ensuring the required system performance is obtained with the minimum of FPGA resource.



These models also demonstrate the excellent characteristics obtained using RFEL's fixed-point cores, without the need for resource-inefficient floating-point architectures.

OPTIONAL ITEMS

RFEL is an off-the-shelf IP supplier and designer of front-end RF signal processing solutions. Please do not hesitate to contact us for information on any of the optional items listed below:-

Fixed-point to floating-point output converter
Distributed Half-Band Filters
NCO down-converters
Highly optimised FIR filters using canonical signed digit multiplier techniques.
Multi-channel input interleavers
Multi-channel output de-interleavers
Front-end windowing - see Ventrix Polyphase DFT range

LICENSING AGREEMENTS

The designs are provided in netlist form on a per-use licence basis. A single use licence can be purchased for prototype designs and then upgraded to a higher number of uses at a later date. Standard price breaks are set at 1, 10, 50 and 100 uses. Quantities above 100 uses are negotiated on an individual basis. Prices start from \$3000.

The prices for standard cores assume that the design will fit comfortably into the chosen FPGA and it is a single FPGA solution. For designs that require two or more FPGAs or to be supplied as a bit-stream there will be a nominal non-recurring engineering charge to produce the cores.



CASE STUDIES

The following examples illustrate the resource usage, complex data rate and an estimate of the typical power consumption. Different size transforms, precision options and target devices have been selected to provide comprehensive illustrations of expected core performance.

Case #1 Part No. Vectis-HS-R2-128K-XV2P-6-14-17-31-H.

Case Study 1 is for a 128k-points PFFT, with input bit-width of 14, twiddle bit-width of 17 and high precision (1 bit growth per stage). No input Buffer or Bit Reversal functions have been included in the core, so as to achieve the maximum size PFFT possible for realistic design requirements when targeted at a large Xilinx Virtex-II PRO, -6 speed grade device, xc2vp70-6fg1517.

Place and Route Report Showing Silicon Usage

Release 6.2.02i Map G.30
Xilinx Mapping Report File for Design 'vectis_hs_rad2_fft_core'

Design Information

Command Line : map -u -p xc2vp70-6ff1517 vectis_hs_rad2_fft_core.ngd -o
vectis_hs_rad2_fft_core_map.ncd vectis_hs_rad2_fft_core.pcf
Target Device : x2vp70
Target Package : ff1517
Target Speed : -6
Stepping Level : 1
Mapper Version : virtex2p -- \$Revision: 1.16.8.1 \$
Mapped Date : Thu May 13 12:25:41 2004

Design Summary

Number of errors: 0
Number of warnings: 236
Logic Utilization:
Number of Slice Flip Flops: 7,316 out of 66,176 11%
Number of 4 input LUTs: 3,670 out of 66,176 5%
Logic Distribution:
Number of occupied Slices: 5,078 out of 33,088 15%
Number of Slices containing only related logic: 5,078 out of 5,078 100%
Number of Slices containing unrelated logic: 0 out of 5,078 0%
*See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs: 6,466 out of 66,176 9%
Number used as logic: 3,670
Number used as a route-thru: 822
Number used as Shift registers: 1,974

Number of PPC405s: 0 out of 2 0%
Number of Block RAMs: 324 out of 328 98%
Number of MULT18X18s: 26 out of 328 7%
Number of GTs: 0 out of 20 0%
Number of GT10s: 0 out of 0 0%

Total equivalent gate count for design: 21,559,776
Peak Memory Usage: 302 MB



NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs. When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Timing

Timing errors: 0 Score: 0

Constraints cover 95949 paths, 0 nets, and 36774 connections

Design statistics:

Minimum period: 7.496ns (Maximum frequency: 133.404MHz)
Maximum path delay from/to any node: 7.496ns

From the maximum clock frequency of 133MHz and noting the interleaved complex input data format required for a Vectis 'HiSpeed' core, refer to FFT Input Formats, the maximum ADC sample rate is also 133MS/s i.e. twice the complex sample frequency, 2fs.

Power Requirements

The following figures were generated using the Xilinx Virtex-II Pro Power Estimate Worksheet V1.2.0.

Total Core Power

Table with 3 columns: Target Device, Target Package, Total Estimated Design Power (mW). Row 1: XC2VP70, FF1517, 11,425

CLB Logic Power

Table with 9 columns: Name, Frequency (MHz), Total Number of CLB Slices, Total Number of Flip/Flop or Latches, Total Number of Shift Register LUTs, Total Number of Select RAM LUTs, Average Toggle Rate %, Amount of Routing Used, VCCint Subtotal (mW). Row 1: User Module 1, 133, 5078, 7316, 1974, 0, 50%, Medium, 2850

**Block RAM Power**

Name	Total Number of BlockRAM Cells	Port A Frequency (MHz)	Port A Width	Port A Read Rate %	Port A Write Rate %	Port B Frequency (MHz)	Port B Width	Port B Read Rate %	Port B Write Rate %	VCCint Subtotal (mW)
User Module 1	324	133	18	0%	100%	133	18	100%	0%	6838

Block Multiplier Power

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %	VCCint Subtotal (mW)
User Module 1	26	133	Medium	570

Assumptions

Average Toggle rate is set to 50%, as all of core runs at the clock rate. Random data has a 50% toggle rate and a pessimistic view would be that the whole core is dedicated to the processing of random data.

In addition an assumption is made that all Block RAM elements are 18-bit. In reality some will be less and some will be greater, with wider delays being constructed of several narrow RAM structures in parallel.



Case #2 Part No. Vectis-HS-R2-1024-XV2P-6-12-17-19-S-IB-BR.

Case Study 2 is for a 1k-point PFFT, with input bit-width of 12, twiddle bit-width of 17 and Single multiplier precision (1 bit growth per stage, up to 17 bits then fixed until last two stages). Input Buffer and Bit Reversal functions have been included in the core, so as to achieve the maximum functionality for the PFFT possible for realistic design requirements when targeted at a small Xilinx Virtex-II PRO, -6 speed grade device, xc2vp4-6fg456.

Place and Route Report Showing Silicon Usage

Release 6.2.02i Map G.30

Xilinx Mapping Report File for Design 'vectis_hs_rad2_fft_core'

Design Information

Command Line : map -u -p xc2vp4-6fg456 vectis_hs_rad2_fft_core.ngd -o
vectis_hs_rad2_fft_core_map.ncd vectis_hs_rad2_fft_core.pcf
Target Device : x2vp4
Target Package : fg456
Target Speed : -6
Stepping Level : 1
Mapper Version : virtex2p -- \$Revision: 1.16.8.1 \$
Mapped Date : Tue May 11 17:07:26 2004

Design Summary

Number of errors: 0
Number of warnings: 132
Logic Utilization:
Number of Slice Flip Flops: 3,193 out of 6,016 53%
Number of 4 input LUTs: 1,831 out of 6,016 30%
Logic Distribution:
Number of occupied Slices: 2,356 out of 3,008 78%
Number of Slices containing only related logic: 2,356 out of 2,356 100%
Number of Slices containing unrelated logic: 0 out of 2,356 0%
*See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs: 3,012 out of 6,016 50%
Number used as logic: 1,831
Number used as a route-thru: 351
Number used as Shift registers: 830

Number of PPC405s: 0 out of 1 0%
Number of Block RAMs: 12 out of 28 42%
Number of MULT18X18s: 8 out of 28 28%
Number of GTs: 0 out of 4 0%
Number of GT10s: 0 out of 0 0%

Total equivalent gate count for design: 914,583
Peak Memory Usage: 127 MB

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs. When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.



Unrelated logic shares no connectivity. Map will only begin packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Timing

Timing errors: 0 Score: 0

Constraints cover 31413 paths, 0 nets, and 13602 connections

Design statistics:

Minimum period: 4.477ns (Maximum frequency: 223.364MHz)
Maximum path delay from/to any node: 4.471ns

From the maximum clock frequency of approximately 223.3 MHz and noting the interleaved complex input data format required for a Vectis 'HiSpeed' core, refer to FFT Input Formats, the maximum ADC sample rate is also 223.3MS/s i.e. twice the complex sample frequency, 2fs.

Power Requirements

The following figures were generated using the Xilinx Virtex-II Pro Power Estimate Worksheet V1.2.0.

Total Core Power

Table with 3 columns: Target Device, Target Package, Total Estimated Design Power (mW). Row 1: XC2VP4, FG456, 3,430

CLB Logic Power

Table with 9 columns: Name, Frequency (MHz), Total Number of CLB Slices, Total Number of Flip/Flop or Latches, Total Number of Shift Register LUTs, Total Number of Select RAM LUTs, Average Toggle Rate %, Amount of Routing Used, VCCint Subtotal (mW). Row 1: User Module 1, 223, 2356, 3193, 830, 0, 50%, Medium, 2071

Block RAM Power

Table with 11 columns: Name, Total Number of BlockRAM Cells, Port A Frequency (MHz), Port A Width, Port A Read Rate %, Port A Write Rate %, Port B Frequency (MHz), Port B Width, Port B Read Rate %, Port B Write Rate %, VCCint Subtotal (mW). Row 1: User Module 1, 12, 223, 18, 0%, 100%, 223, 18, 100%, 0%, 423

**Block Multiplier Power**

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %	VCCint Subtotal (mW)
User Module 1	8	223	Medium	294

Assumptions

Average Toggle rate is set to 50%, as all of core runs at the clock rate. Random data has a 50% toggle rate and a pessimistic view would be that the whole core is dedicated to the processing of random data.



Case #3 Part No. Vectis-HS-R2-1024-SP3-5-12-17-19-S-IB-BR.

Case Study 3 is also for a 1k-point PFFT, in this case the input bit-width is 12, twiddle bit-width is 17 and Single multiplier precision (1 bit growth per stage, up to 17 bits then fixed until last two stages). Input Buffer and Bit Reversal functions have been included in the core, so as to achieve the maximum functionality for the PFFT possible for realistic design requirements when targeted at a medium Xilinx Spartan-3, -5 speed grade device, x3sp400-5fg456.

Place and Route Report Showing Silicon Usage

Release 6.2.02i Map G.30
Xilinx Mapping Report File for Design 'vectis_hs_rad2_fft_core'

Design Information

Command Line : map -u -p xc3s400-5fg456 vectis_hs_rad2_fft_core.ngd -o
vectis_hs_rad2_fft_core_map.ncd vectis_hs_rad2_fft_core.pcf
Target Device : x3s400
Target Package : fg456
Target Speed : -5
Stepping Level : 1
Mapper Version : spartan3 -- \$Revision: 1.16.8.1 \$
Mapped Date : Wed May 12 10:55:37 2004

Design Summary

Number of errors: 0
Number of warnings: 132
Logic Utilization:
Number of Slice Flip Flops: 3,193 out of 7,168 44%
Number of 4 input LUTs: 1,831 out of 7,168 25%
Logic Distribution:
Number of occupied Slices: 2,355 out of 3,584 65%
Number of Slices containing only related logic: 2,355 out of 2,355 100%
Number of Slices containing unrelated logic: 0 out of 2,355 0%
*See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs: 3,012 out of 7,168 42%
Number used as logic: 1,831
Number used as a route-thru: 351
Number used as Shift registers: 830
Number of Block RAMs: 12 out of 16 75%
Number of MULT18X18s: 8 out of 16 50%

Total equivalent gate count for design: 914,583
Peak Memory Usage: 113 MB

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs. When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.



Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Timing

Timing errors: 0 Score: 0

Constraints cover 30586 paths, 0 nets, and 11692 connections

Design statistics:

Minimum period: 6.530ns (Maximum frequency: 153.139MHz)
Maximum path delay from/to any node: 6.479ns

From the maximum clock frequency of approximately 153 MHz and noting the interleaved complex input data format required for a Vectis 'HiSpeed' core, refer to FFT Input Formats, the maximum ADC sample rate is also 153MS/s i.e. twice the complex sample frequency, 2fs.

Power Requirements

The following figures were generated using the Xilinx Spartan-3 Power Estimate Worksheet V1.0.0.

Total Core Power

Table with 3 columns: Target Device (XC3S400), Target Package (FG456), Total Estimated Design Power (mW) (1,309)

CLB Logic Power

Table with 9 columns: Name, Frequency (MHz), Total Number of CLB Slices, Total Number of Flip/Flop or Latches, Total Number of Shift Register LUTs, Total Number of Select RAM LUTs, Average Toggle Rate %, Amount of Routing Used, VCCint Subtotal (mW)

Block RAM Power

Table with 11 columns: Name, Total Number of BlockRAM Cells, Port A Frequency (MHz), Port A Width, Port A Read Rate %, Port A Write Rate %, Port B Frequency (MHz), Port B Width, Port B Read Rate %, Port B Write Rate %, VCCint Subtotal (mW)



Block Multiplier Power

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %	VCCint Subtotal (mW)
User Module 1	8	153	Medium	148

Assumptions

Average Toggle rate is set to 50%, as all of core runs at the clock rate. Random data has a 50% toggle rate and a pessimistic view would be that the whole core is dedicated to the processing of random data.



ADC	Analogue to Digital Converter
ASIC	Application Specific Integrated Circuit
CLB	Configurable Logic Block
DFT	Discrete Fourier Transform
DHBF	Distributed Half-Band Filter
EDIF	Electronic Data Interchange Format
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
I/O	Input / Output
LSB	Least Significant Bit
MSB	Most Significant Bit
MS/s	Million Samples Per Second
PFT	Pipelined Frequency Transform
PFFT	Pipelined Fast Fourier Transform
RFEL	RF Engines Limited
RTL	Register Transfer Level
RPM	Relationally Placed Macro
UCF	User Constraints File
VHDL	Very High Speed IC Hardware Description Language
VITAL	VHDL Initiative Toward ASIC Libraries

Table 3: Glossary

Please refer to the RFEL web site www.rfel.com for details of PFFT cores under development.

Specifications are subject to change without notice.