



OVERVIEW

This document describes the RFEL Vectis 'QuadSpeed' range of Pipelined FFT (PFFT) cores. The cores process complex input data in continuous real time, with no gaps in the data, at complex data rates in excess of 400MS/s. This document provides details of the cores and design services available from RFEL.

Vectis QuadSpeed cores are intended for use in applications where processing speed is critical and optimum use of available silicon is required. The cores are available for licence in netlist form as a component ready to be combined with customer's own IP or as part of an integrated design from RFEL. Alternatively, where the core is to be the *only* contents of an FPGA, it can be provided as a programming bitstream; in this case RFEL would provide a separate design services contract.

FEATURES

- Continuous real time processing of complex data in excess of 400MS/s
 - Compatible with 800MS/s ADC using RFEL's optional DHBF core
 - Fully pipelined design
 - Targeted at Xilinx and Altera FPGA families
 - 32 to 128K-point versions available (longer lengths by request)
 - Bit-width and bit-growth adjustable at factory
 - Twiddle bit-width adjustable at factory
 - Internal memory partitioning adjustable at factory
 - Can be used for real-input FFTs with additional modules
 - Fully bit-true parameterisable models are available
 - Optional input buffer and bit reverser
 - FFT and IFFT functionality
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APPLICATIONS

- Wide-band filter banks
 - Communications systems
 - Electronic warfare (radar, sonar, surveillance)
 - Medical instrumentation
 - Test instrumentation
 - Real-time spectral analysis
 - Multi-channel systems, where many low speed channels are interleaved through the high-speed core.
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GENERAL DESCRIPTION

The Vectis QuadSpeed range is based on a radix-2 Decimation-in-Frequency (DIF) pipelined FFT. The architecture is based on 'n' successive stages, where 2^n is the size of the FFT. Each stage has switched delay elements and butterflies. The switches and delays of each stage re-order the data into the correct order for processing by the butterfly. There are 'n' butterflies, each performing a 2-point Discrete Fourier Transform (DFT) and complex phase rotations (twiddles). Figure 1 below shows the basic architecture of the cores.

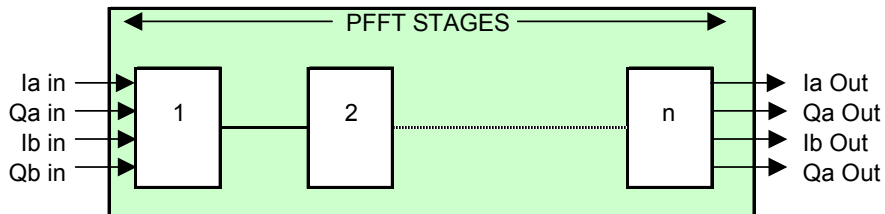


Figure 1: Vectis QuadSpeed n-point PFFT

EXAMPLES USED IN THIS DOCUMENT

To limit the diagrams to a convenient size, a 32-point PFFT is used in the examples below.

FFT INPUT FORMATS

FFT with Input Buffer

The PFFT core can be supplied with an optional Input Buffer that formats the data as required for the PFFT function. With this configuration simple de-interleaving of the complex input data is required prior to input to the PFFT core. The format of the PFFT data input is signed 2's-complement as shown in Figure 2 below.

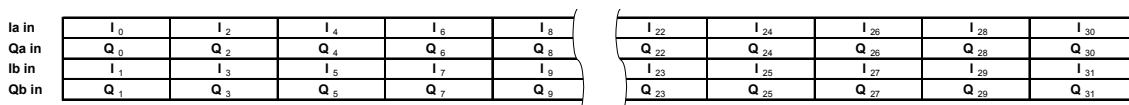


Figure 2: 32-point PFFT Data Input Format Example with Input Buffer Included

'Ia', 'Qa', 'Ib' and 'Qb' show the 32 de-interleaved time-ordered complex data samples required to be input at a frequency of $f_s/2$, where f_s is the original complex sample frequency.

The PFFT core is clocked at $f_s/2$.

FFT without Input Buffer

If the PFFT core is supplied with no Input Buffer option selected then the input data must be re-ordered, as shown in Figure 3. The PFFT core is clocked at the same rate as the input data of $f_s/2$.

la in	I ₀	I ₁	I ₂	I ₃	I ₄	I ₁₁	I ₁₂	I ₁₃	I ₁₄	I ₁₅
Qa in	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₁₁	Q ₁₂	Q ₁₃	Q ₁₄	Q ₁₅
lb in	I ₁₆	I ₁₇	I ₁₈	I ₁₉	I ₂₀	I ₂₇	I ₂₈	I ₂₉	I ₃₀	I ₃₁
Qb in	Q ₁₆	Q ₁₇	Q ₁₈	Q ₁₉	Q ₂₀	Q ₂₇	Q ₂₈	Q ₂₉	Q ₃₀	Q ₃₁

Figure 3: 32-point PFFT Data Input Format Example with No Input Buffer Included

FFT OUTPUT FORMATS

FFT with Bit Reverser

The PFFT core can be supplied with an optional Bit Reverser that reorders the complex frequency samples to be in the time order shown in Figure 4 below. The format of the PFFT core data output is signed 2's-complement. This format can be converted to other formats by the addition of separate modules available from RFEL.

Data is output at the PFFT core clock rate of $f_s/2$, where f_s is the complex sample rate.

la out	I ₀	I ₁	I ₂	I ₃	I ₄	I ₁₁	I ₁₂	I ₁₃	I ₁₄	I ₁₅
Qa out	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₁₁	Q ₁₂	Q ₁₃	Q ₁₄	Q ₁₅
lb out	I ₁₆	I ₁₇	I ₁₈	I ₁₉	I ₂₀	I ₂₇	I ₂₈	I ₂₉	I ₃₀	I ₃₁
Qb out	Q ₁₆	Q ₁₇	Q ₁₈	Q ₁₉	Q ₂₀	Q ₂₇	Q ₂₈	Q ₂₉	Q ₃₀	Q ₃₁

Figure 4: 32-point PFFT Data Output with Bit Reverser

FFT without Bit Reverser

If the PFFT core with no Bit Reverser option is selected then the output complex frequency samples are in a bit-reversed time order as shown in Figure 5 below.

Data is output at the PFFT core clock rate of $f_s/2$, where f_s is the complex sample rate.

la out	I ₀	I ₈	I ₄	I ₁₂	I ₃	I ₁₁	I ₇	I ₁₅
Qa out	Q ₀	Q ₈	Q ₄	Q ₁₂	Q ₃	Q ₁₁	Q ₇	Q ₁₅
lb out	I ₁₆	I ₂₄	I ₂₀	I ₂₈	I ₁₉	I ₂₇	I ₂₃	I ₃₁
Qb out	Q ₁₆	Q ₂₄	Q ₂₀	Q ₂₈	Q ₁₉	Q ₂₇	Q ₂₃	Q ₃₁

Figure 5: 32-point PFFT Data Output with No Bit Reverser

Frequency Sample Output Centre Frequency

For the 32 sample PFFT example, the centre frequency of each complex frequency sample is given by the following equation: -

$$\text{Bin Frequency}(n) = n * f_s / 32$$

Where n is the complex output frequency sample number in the range 0 to 31, and f_s is the original complex sample frequency.

Or in general terms, $\text{Bin Frequency}(n) = n * f_s / \text{FFT_size}$

CLOCK ENABLE FUNCTION

The PFFT also facilitates the processing of data at a reduced rate with the use of a clock enable signal, 'c_en'. This signal is active when asserted with logic '1' to validate input data samples, and can either be 'strobed' for reduced data rate applications or tied active.

This signal can be used as a true clock enable where data is input at a reduced rate from that of the available core clock, a typical example would be after the de-multiplexing and formatting of the complex data as per the input format requirements of the QuadSpeed PFFT core illustrated in Figure 2. This technique will only be practical with clock rates in the order of 200MHz; beyond that clock division to accompany the data is the recommended technique.

The second application of the 'c_en' signal is for use as a sample enable. This is useful in systems where cross clock domains are required to capture the digitised data, resulting in data accompanied with a 'data-valid' identifier, but not in a periodic nature with empty or null data samples. This 'data-valid' identifier can be connected to the 'c_en' input.

In both cases if the 'c_en' signal is used, the output signal 'c_en_out' should be used as the enable to validate the output samples from the PFFT. This is important as the distribution of the 'c_en' signal within the core causes a clock period of delay. The 'c_en_out' signal accounts for this and maintains the alignment of the 'c_en' with the output samples.

Figure 6 illustrates the use of the 'c_en' signal, specifically as a sample enable.

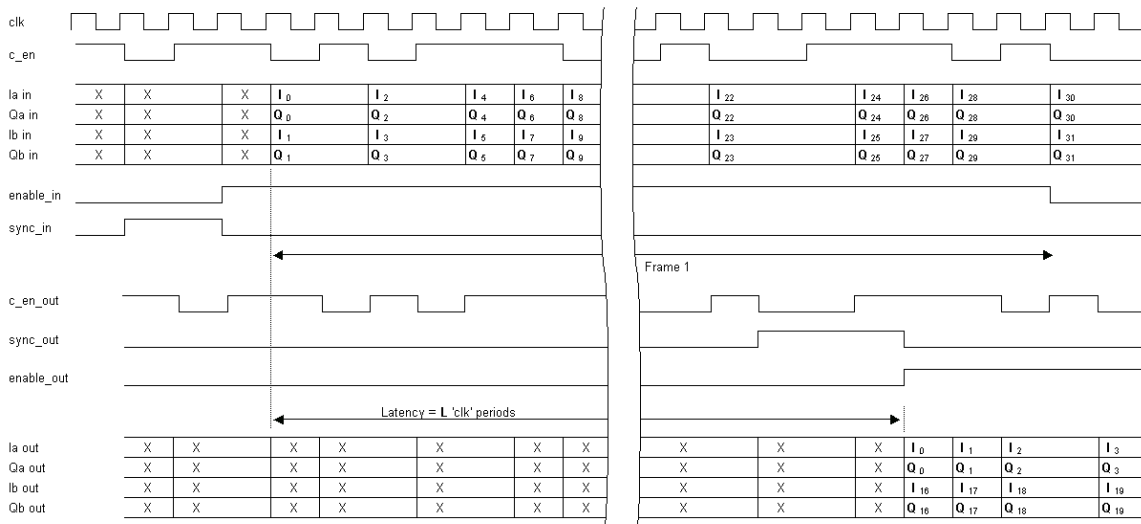


Figure 6: Illustration of clock enable function

N.B. For clarity all subsequent diagrams assume that the 'c_en' signal is tied to logic '1' and data samples are at the core clock rate.

CORE INPUT SYNCHRONISATION

The PFFT can process input data blocks continuously (back to back with no gaps in time) or as discrete time separated blocks. In either case, the core requires the active high 'sync_in' signal to

be active for one clock period, two clock periods prior to the first complex sample. It also requires the active high 'enable_in' signal to be asserted for a duration equal to the PFFT block size; one clock period prior to the first complex sample, as shown in the 32-point timing diagram example of Figure 7 below.

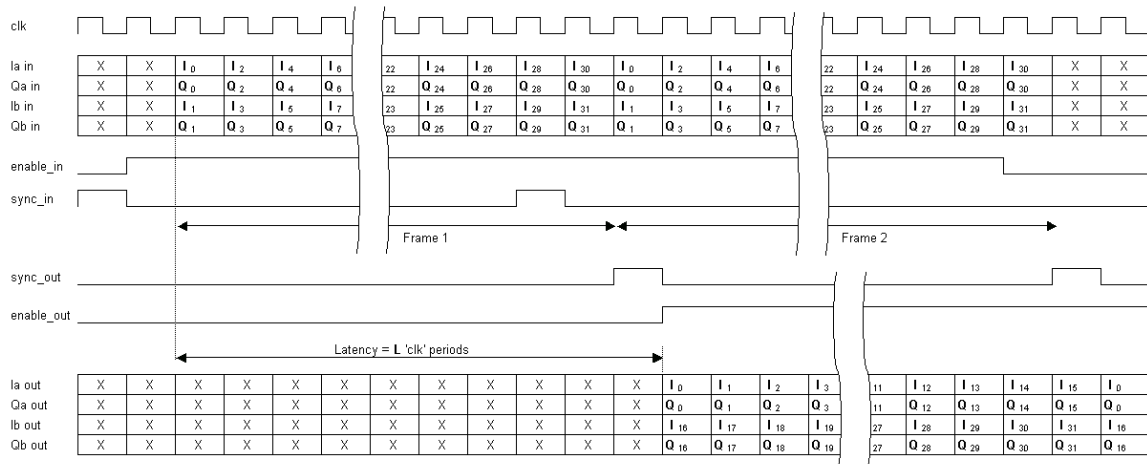


Figure 7: 32-point PFFT I/O Timing Diagram Example

CORE OUTPUT SYNCHRONISATION

The first complex sample of each output block is marked by the active-high 'sync_out', one clock period prior to the first complex sample. The active high 'enable_out' signal is also asserted for a duration equal to the PFFT block size; coincident with the first complex sample as shown in the timing diagram example of Figure 7.

Figure 7 is illustrated showing a PFFT core combination with Input Buffer and Bit Reverser present. The relative timing of input control with respect to the data and output control with respect to the data signals is the same for all combinations of PFFT core with or without Input Buffer and Bit Reverser. The latency however is different for each of these options, as described later.

IFFT OUTPUT

The PFFT core is also able to produce an IFFT computation. This is controlled using the core input 'fft_ifft' and allows the output sample sequence to be either: -

- FFT of input complex samples when 'fft_ifft' is logic '1'
- IFFT of input complex samples when 'fft_ifft' is logic '0'

It is important to note that the 'fft_ifft' signal is intended to be a 'static' input. If 'fft_ifft' is changed while the PFFT core is processing data, then several blocks of data will be output incorrectly. The number of 'corrupt' blocks will be dependent on the pipeline latency of the PFFT core.



LATENCY

Latency is defined in this datasheet as the time from when the first complex sample of an input block is clocked into the PFFT to the time when the first transformed complex frequency output sample is clocked out from the PFFT. This is shown in the timing diagram example of Figure 7 above. The latency can be calculated by:

$$'L' = [1 + (t_{ib} + t_{fft} + t_{area} + t_{br}) * t_{c_en}] \text{ PFFT core clock periods.}$$

Where

1 = distribution delay of clock enable input, 'c_en'

t_{ib} = input_buffer_present x (N/4 + 3)

t_{fft} = N/2 + 10 x log₂(N) – 13

t_{area} = area_option_selected x log₂(N) – 2

t_{br} = (N/2 - 2^{⌊log₂(N/2) / 2⌋} - 2^{⌊log₂(N/2) + 1 / 2⌋} + 10) x bit_reverser_present

t_{c_en} = 1/duty_cycle

'N' is the FFT length

'input_buffer_present', when PFFT core has the Input Buffer function included assign a value of 1 to include it's latency else assign a value of 0.

'bit_reverser_present', when PFFT core has the Bit Reverser function included assign a value of 1 to include it's latency else assign a value of 0.

'area_option_selected', when true, implements an alternative arithmetic unit to reduce the use of multiplier resource. This option is a factory-selected option that depends on the maximum sample rate required and the available resource. Assign a value of 1 to include its additional latency else assign a value of 0.

'duty_cycle', when 'c_en' tied to logic '1' the core is permanently clock enabled, else the clock enable is active at some rate – this is the duty cycle. For a sample enable option were period is random, the exact latency cannot be determined, only an average based on the average duty-cycle of 'c_en'.

For the 32 sample PFFT example, with 33.3% duty cycle enable and assuming a combination of input buffer present and bit reverser present and no area option: -

$$'L' = 1 + [(8 + 3) + (32/2 + 10 \times 5 - 13) + 0 + (16 - 4 - 4 + 10)] * 1/0.33$$

$$'L' = 247 \text{ PFFT core clocks.}$$

The PFFT core is a continuous pipeline, so valid data is continuously available at the output after the initial delay due to the pipeline filling up.



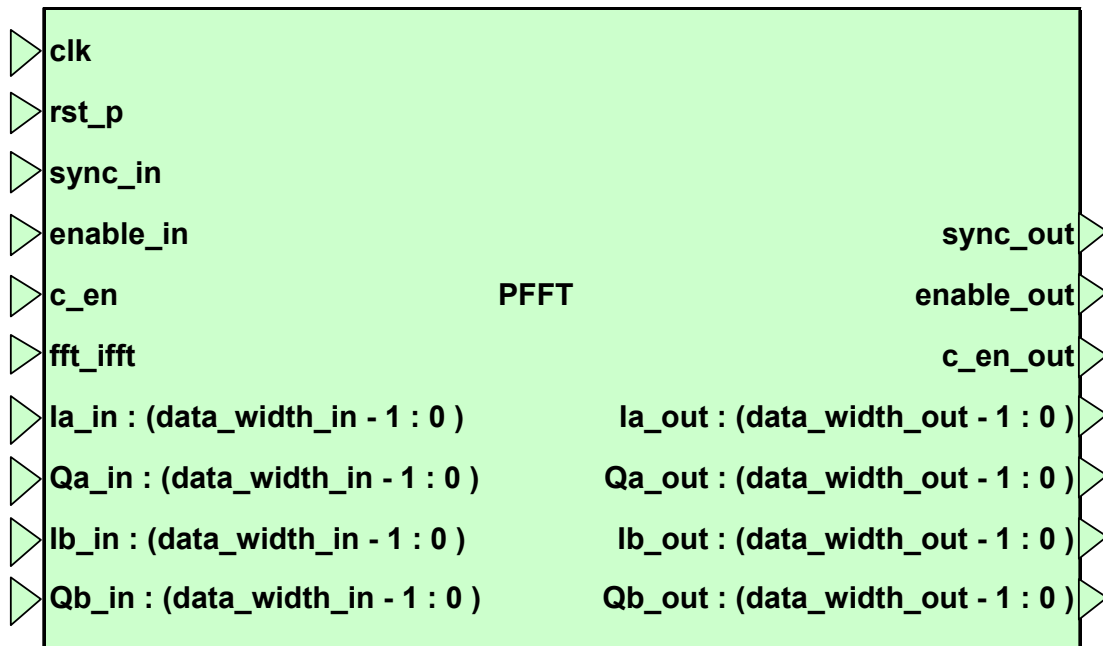
CORE INTERFACE DESCRIPTION

All core inputs should be synchronised to the 'clk' signal. All core outputs are synchronised by the 'clk' signal.

Signal	Direction	Type	Width	Function
clk	IN	Std logic	1 bit	The core clock rate is equal to $f_s/2$. Where f_s is the complex input rate.
c_en	IN	Std logic	1 bit	Input clock enable. Active-high signal, one clock period in duration, for each valid input sample.
rst_p	IN	Std logic	1 bit	An active-high pulse, of duration greater than 2 core clock enable periods, resets the PFFT control logic, but not the PFFT pipeline.
sync_in	IN	Std logic	1 bit	Active-high pulse marking the first sample of a new input block. Precedes first samples of complex input data by two clock enable periods.
enable_in	IN	Std logic	1 bit	Active-high signal asserted for a duration equal to the PFFT block length. Asserted one clock enable period before the first samples of complex input data.
fft_ifft	IN	Std logic	1 bit	Active-high signal to select FFT function, else an IFFT function is performed.
la_in, Qa_in, lb_in, Qb_in	IN	Std logic vector	(data_width_in - 1 downto 0)	2's complement time-domain data.
sync_out	OUT	Std logic	1 bit	Active-high pulse marking the first transformed sample of a new output block. Asserted one clock enable period before the first transformed samples of a new output block.
c_en_out	OUT	Std logic	1 bit	Output clock enable. Active-high signal, one clock period in duration, for each valid output sample.
enable_out	OUT	Std logic	1 bit	Active-high signal asserted for the duration of to the PFFT block length. Coincident with the first transformed samples of a new output block.
la_out, Qa_out, lb_out, Qb_out	OUT	Std logic vector	(data_width_out - 1 downto 0)	2's complement frequency-domain data.

Table 1: PFFT Interface Specification

N.B. A reduction in core power can be obtained by inhibiting the 'sync_in' or the 'c_en' signal. Inhibiting the 'sync_in' will allow the pipeline to flush, whilst inhibiting the 'c_en' will stop the PFFT immediately. This power-save mode can be used whenever the core is not required to operate in continuous mode.


Figure 8: PFFT Symbol

POWER REQUIREMENTS

The power requirement for any particular core will be highly dependent on the target device, size of implementation, and clock rate. RFEL can provide individual power estimates for a particular design if required. See Case Studies for some examples.

VERIFICATION

Verification of the core is achieved in several distinct phases in the design cycle.

Initially, a bit-true Matlab model of the core is used to provide reference output data, using a specific set of input stimuli. These models exactly match the behaviour of the hardware architecture and their outputs are bit-true representations of the actual core.

The input stimuli are used to functionally (pre-synthesis) test the VHDL code using the ModelSim simulator. The results of these simulations are automatically compared with the reference data generated by the bit-true Matlab model and pass/fail indications are reported.

After the VHDL has been synthesised and place-and-route of the core is complete, timing simulations, based on the chip vendor's simulation netlist and gate delay files for the core are performed. These also take the form of the functional tests, but being based on the compiled netlist and timing files from the FPGA vendor, they verify the expected timings of the delivered core.

The bit-true Matlab models are also included.



DELIVERABLES

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL VHDL Model. Bit-true Matlab model and scripts. Placement reports.

Table 2: Items provided with each core

Electronic transfer is used to deliver the cores and supporting documentation.
Optional design support services are available to help you incorporate the core into your design.

INFORMATION REQUIRED FOR QUOTATION

To enable RFEL to provide the required PFFT core, select from the options list below the required parameters and contact us at 'sales@rfel.com'

- Product*^{*1} = Vectis 'HiSpeed' or Vectis 'QuadSpeed'
- Radix* = Currently only Radix 2 available as off the shelf
- CE*^{*2} = Indicates architecture supports clock enable/sample enable functionality.
- Length* = (powers of 2 from 8 through 131072)
- Target technology*
 - 'XV2P' = Xilinx Virtex-II PRO
 - 'AS' = Altera Stratix
 - 'AS2' = Altera Stratix2
 - 'XV2' = Xilinx Virtex-II
 - 'SP3' = Xilinx Spartan3
- Speed grade* = technology specific '6 for example'
- Input bit-width* = 8 to 22 bits
- Twiddle bit-width*^{*3} = 10 to 18 bits
- Output bit-width* = 8 to 32 bits
- Precision*
 - H = High Precision (1 bit growth per stage).
 - S = Single Multiplier (17 bits used at each stage),
 - U = user definable (defined prior to order).
- IB* = Input buffer included in core
- BR* = Bit-reverser included in core.

^{*1}Data sheet is for QuadSpeed product only.
^{*2}The QuadSpeed product supports clock enable function as standard.
^{*3}Larger twiddle widths are available, but will increase size/reduce speed.

In addition, *f_s*, *Max Complex Input Sample Rate* will need to specified



For examples of the product part number required for order refer to the Case Studies section.

ARITHMETIC PRECISION OPTIONS

The arithmetic precision used within an FFT core will determine the accuracy of the results. The Vectis range of Pipelined FFT cores allows the arithmetic precision of each butterfly stage to be specified to provide an optimal solution in terms of silicon and performance.

The three precision options offered are described below: -

H (High Precision) Growing the arithmetic precision by one bit per radix-2 stage is generally more than most systems require, but it provides the best spurious free performance, system noise level and magnitude and phase accuracies. Obviously this option will lead to a larger implementation compared with one that is tightly tailored to the performance requirements of the system. In many cases, the hardware overhead is not significant (see Case Study 'Virtex II PRO and Spartan3 Placed and Routed Device Utilisation and Maximum Clock Rate).

S (Single Multiplier Precision) The Virtex-II / PRO, Spartan3 and Altera Stratix architectures contain 18-bit x 18-bit signed multiplier blocks. This precision option ensures that only four of these multiplier blocks are required for each butterfly stage rather than the 8 or even 16 blocks that would be required for stage/twiddle bit widths of 18-bits and over. The result is a core that is optimal in terms of logic and multiplier resource, but has a limited spurious free performance and magnitude and phase accuracy.

U (User-Defined Precision) This option allows the core to be optimised to meet the user's system performance requirements with the minimum of silicon.

RFEL has extensive experience and a range of analysis tools that allow us to assess bit-true system performance. Parameters such as spurious free dynamic range, system noise characteristics, magnitude and phase accuracy, etc. can be measured for various arithmetic precisions, to allow an optimal solution to be developed.

RFEL offer parameterisable bit-true models that match the behaviour of our cores exactly. These models allow system engineers to investigate the precision trade-offs within their own system before ordering.

The maximum input range of the 'QuadSpeed cores' is determined by input bit width and is given using the formula $(2^{(\text{input_bit_width} - 1)} - 1)$.

ENGINEERING SUPPORT SERVICES AND MODELS

Accuracy and precision are system design considerations that affect data and twiddle bit-widths. RFEL can offer system-engineering advice to aid the selection of the optimal core configuration.

RFEL also offer system-engineering advice to assist in the selection of an optimal core for the system requirement. For example accuracy, precision and spurious free dynamic range/noise floor can all be modelled using Matlab bit-true models. This ensures input and output bit-widths, twiddle



bit-width and arithmetic bit growth at each stage can all be optimised, ensuring the required system performance is obtained with the minimum of FPGA resource.

These models also demonstrate the excellent characteristics obtained using RFEL's fixed-point cores, without the need for resource-inefficient floating-point architectures.

OPTIONAL ITEMS

RFEL is an off-the-shelf IP supplier and designer of front-end RF signal processing solutions. Please do not hesitate to contact us for information on any of the optional items listed below: -

Fixed-point to floating-point output converter
Distributed Half-Band Filters
NCO down-converters
Highly optimised FIR filters using canonical signed digit multiplier techniques.
Multi-channel input interleavers
Multi-channel output de-interleavers
Front-end windowing - see Ventrrix Polyphase DFT range

LICENSING AGREEMENTS

The designs are provided in netlist form on a per-use licence basis. A single use licence can be purchased for prototype designs and then upgraded to a higher number of uses at a later date. Standard price breaks are set at 1, 10, 50 and 100 uses. Quantities above 100 uses are negotiated on an individual basis. Prices start from \$3000.

The prices for standard cores assume that the design will fit comfortably into the chosen FPGA and it is a single FPGA solution. For designs that require two or more FPGAs or to be supplied as a bit-stream there will be a nominal non-recurring engineering charge to produce the cores.



CASE STUDIES

The following examples illustrate the resource usage, complex data rate and an estimate of the typical power consumption. Different size transforms have been selected to provide comprehensive illustrations of expected core performance.

Case #1 Part No. Vectis-QS-R2-CE-16384-XV2P-6-12-18-26-H-IB-BR.

Case Study 1 is for a 16k-point PFFT, with input bit-width of 12, twiddle bit-width of 18 and high precision (1 bit growth per stage). Input Buffer and Bit Reversal functions are included in the core. The design is targeted at the large Xilinx Virtex-II PRO, -6 speed grade device: xc2vp30-6fg676.

Place and Route Report Showing Silicon Usage

Release 6.2.02i Map G.30
Xilinx Mapping Report File for Design 'vectis_qs_rad2_fft_core'

Design Information

Command Line : map -u -p xc2vp30-6fg676 vectis_qs_rad2_fft_core.ngd -o

vectis_qs_rad2_fft_core_map.ncd vectis_qs_rad2_fft_core.pcf

Target Device : x2vp30
Target Package : fg676
Target Speed : -6
Stepping Level : 1
Mapper Version : virtex2p -- \$Revision: 1.16.8.1 \$
Mapped Date : Wed Oct 06 11:45:31 2004

Design Summary

Number of errors: 0
Number of warnings: 292
Logic Utilization:
Number of Slice Flip Flops: 13,158 out of 27,392 48%
Number of 4 input LUTs: 7,240 out of 27,392 26%
Logic Distribution:
Number of occupied Slices: 7,939 out of 13,696 57%
Number of Slices containing only related logic: 7,939 out of 7,939 100%
Number of Slices containing unrelated logic: 0 out of 7,939 0%
*See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs: 9,630 out of 27,392 35%
Number used as logic: 7,240
Number used as a route-thru: 857
Number used as Shift registers: 1,533

Number of PPC405s: 0 out of 2 0%
Number of Block RAMs: 120 out of 136 88%
Number of MULT18X18s: 52 out of 136 38%
Number of GTs: 0 out of 8 0%
Number of GT10s: 0 out of 0 0%

Total equivalent gate count for design: 8,347,563



Peak Memory Usage: 293 MB

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs. When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Timing

Timing errors: 4 Score: 500

Constraints cover 143013 paths, 0 nets, and 50067 connections

Design statistics:

Minimum period: 5.228ns (Maximum frequency: 191.278MHz)

Maximum path delay from/to any node: 4.995ns

From the maximum clock frequency of 191MHz and noting the parallel complex input data format required for a Vectis 'QuadSpeed' core with this configuration, refer to FFT Input Formats, the maximum complex sample rate that can be processed is greater than 382MS/s.

It should be noted that when this core is placed within a registered design 200MHz clock frequency, and hence complex sample rate of 400MHz, is achieved.

Power Requirements

The following figures were generated using the Xilinx Virtex-II Pro Power Estimate Worksheet V1.2.0.

Total Core Power

Target Device	Target Package	Total Estimated Design Power (mW)
XC2VP30	FG676	6741.6667

CLB Logic Power

Name	Frequency (MHz)	Total Number of CLB Slices	Total Number of Flip/Flop or Latches	Total Number of Shift Register LUTs	Total Number of Select RAM LUTs	Average Toggle Rate %	Amount of Routing Used	VCCint Subtotal (mW)
User Module 1	200	7939	13158	1533	0	50%	Medium	2965

**Block RAM Power**

Name	Total Number of BlockRAM Cells	Port A Frequency (MHz)	Port A Width	Port A Read Rate %	Port A Write Rate %	Port B Frequency (MHz)	Port B Width	Port B Read Rate %	Port B Write Rate %	VCCint Subtotal (mW)
User Module 1	120	200	18	0%	100%	200	18	100%	0%	1902

Block Multiplier Power

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %	VCCint Subtotal (mW)
User Module 1	52	200	Medium	858

Assumptions

Average Toggle rate is set to 50%, as it is assumed that the entire core is run at the clock rate in the above configuration with the 'c_en' input tied to logic '1'. Random data has a 50% toggle rate, and a pessimistic view would be that the whole core is dedicated to the processing of random data.

In addition an assumption is made that all Block RAM elements are 18-bit. In reality some will be less and some will be greater, with wider delays being constructed of several narrow RAM structures in parallel.



Case #2 Part No. Vectis-QS-R2-CE-1024-XV2P-6-16-18-26-H-IB-BR.

Case Study 2 is for a 1k-point PFFT, with input bit-width of 16, twiddle bit-width of 18 and high precision (1 bit growth per stage). Input Buffer and Bit Reversal functions are included in the core. The design is targeted at a medium Xilinx Virtex-II PRO, -6 speed grade device: xc2vp20-6fg676.

Place and Route Report Showing Silicon Usage

Release 6.2.02i Map G.30

Xilinx Mapping Report File for Design 'vectis_qs_rad2_fft_core'

Design Information

Command Line : map -u -p xc2vp20-6fg676 vectis_qs_rad2_fft_core.ngd -o

vectis_qs_rad2_fft_core_map.ncd vectis_qs_rad2_fft_core.pcf

Target Device : x2vp20

Target Package : fg676

Target Speed : -6

Stepping Level : 1

Mapper Version : virtex2p -- \$Revision: 1.16.8.1 \$

Mapped Date : Wed Oct 06 15:26:43 2004

Design Summary

Number of errors: 0

Number of warnings: 307

Logic Utilization:

Number of Slice Flip Flops: 10,492 out of 18,560 56%

Number of 4 input LUTs: 5,187 out of 18,560 27%

Logic Distribution:

Number of occupied Slices: 6,068 out of 9,280 65%

Number of Slices containing only related logic: 6,068 out of 6,068 100%

Number of Slices containing unrelated logic: 0 out of 6,068 0%

*See NOTES below for an explanation of the effects of unrelated logic

Total Number 4 input LUTs: 6,612 out of 18,560 35%

Number used as logic: 5,187

Number used as a route-thru: 542

Number used as Shift registers: 883

Number of PPC405s: 0 out of 2 0%

Number of Block RAMs: 18 out of 88 20%

Number of MULT18X18s: 40 out of 88 45%

Number of GTs: 0 out of 8 0%

Number of GT10s: 0 out of 0 0%

Total equivalent gate count for design: 1,531,705

Peak Memory Usage: 231 MB

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs.

When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin



packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Timing

Timing errors: 0 Score: 0

Constraints cover 106991 paths, 0 nets, and 34941 connections

Design statistics:

Minimum period: 5.000ns (Maximum frequency: 200.000MHz)
Maximum path delay from/to any node: 4.995ns

From the maximum clock frequency of 200MHz and noting the parallel complex input data format required for a Vectis 'QuadSpeed' core with this configuration, refer to FFT Input Formats, the maximum complex sample rate that can be processed is up to 400MS/s.

Power Requirements

The following figures were generated using the Xilinx Virtex-II Pro Power Estimate Worksheet V1.2.0.

Total Core Power

Table with 3 columns: Target Device, Target Package, Total Estimated Design Power (mW). Row 1: XC2VP20, FG676, 4003.6667

CLB Logic Power

Table with 9 columns: Name, Frequency (MHz), Total Number of CLB Slices, Total Number of Flip/Flop or Latches, Total Number of Shift Register LUTs, Total Number of Select RAM LUTs, Average Toggle Rate %, Amount of Routing Used, VCCint Subtotal (mW). Row 1: User Module 1, 200, 6068, 10492, 883, 0, 50%, Medium, 2192

Block RAM Power

Table with 11 columns: Name, Total Number of BlockRAM Cells, Port A Frequency (MHz), Port A Width, Port A Read Rate %, Port A Write Rate %, Port B Frequency (MHz), Port B Width, Port B Read Rate %, Port B Write Rate %, VCCint Subtotal (mW). Row 1: User Module 1, 18, 200, 18, 0%, 100%, 200, 18, 100%, 0%, 285

**Block Multiplier Power**

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %	VCCint Subtotal (mW)
User Module 1	40	200	Medium	660

Assumptions

Average Toggle rate is set to 50%, as it is assumed that the entire core is run at the clock rate in the above configuration with the 'c_en' input tied to logic '1'. Random data has a 50% toggle rate, and a pessimistic view would be that the whole core is dedicated to the processing of random data.

In addition an assumption is made that all Block RAM elements are 18-bit. In reality some will be less and some will be greater, with wider delays being constructed of several narrow RAM structures in parallel.



Case #3 Part No. Vectis-QS-R2-CE-128-XV2P-6-14-18-21-H-IB-BR.

Case Study 3 is for a 128-point PFFT, with input bit-width of 14, twiddle bit-width of 18 and high precision (1 bit growth per stage). Input Buffer and Bit Reversal functions are included in the core. The design is targeted at a small Xilinx Virtex-II PRO, -6 speed grade device: xc2vp4-6ff672.

Place and Route Report Showing Silicon Usage

Release 6.2.02i Map G.30

Xilinx Mapping Report File for Design 'vectis_qs_rad2_fft_core'

Design Information

Command Line : map -u -p xc2vp4-6ff672 vectis_qs_rad2_fft_core.ngd -o

vectis_qs_rad2_fft_core_map.ncd vectis_qs_rad2_fft_core.pcf

Target Device : x2vp4

Target Package : ff672

Target Speed : -6

Stepping Level : 1

Mapper Version : virtex2p -- \$Revision: 1.16.8.1 \$

Mapped Date : Wed Oct 06 16:03:17 2004

Design Summary

Number of errors: 0

Number of warnings: 198

Logic Utilization:

Number of Slice Flip Flops: 5,206 out of 6,016 86%

Number of 4 input LUTs: 2,931 out of 6,016 48%

Logic Distribution:

Number of occupied Slices: 3,006 out of 3,008 99%

Number of Slices containing only related logic: 2,909 out of 3,006 96%

Number of Slices containing unrelated logic: 97 out of 3,006 3%

*See NOTES below for an explanation of the effects of unrelated logic

Total Number 4 input LUTs: 3,890 out of 6,016 64%

Number used as logic: 2,931

Number used as a route-thru: 263

Number used as Shift registers: 696

Number of PPC405s: 0 out of 1 0%

Number of Block RAMs: 12 out of 28 42%

Number of MULT18X18s: 16 out of 28 57%

Number of GTs: 0 out of 4 0%

Number of GT10s: 0 out of 0 0%

Total equivalent gate count for design: 964,815

Peak Memory Usage: 150 MB

NOTES:

Related logic is defined as being logic that shares connectivity - e.g. two LUTs are "related" if they share common inputs.

When assembling slices, Map gives priority to combine logic that is related. Doing so results in the best timing performance.

Unrelated logic shares no connectivity. Map will only begin



packing unrelated logic into a slice once 99% of the slices are occupied through related logic packing.

Note that once logic distribution reaches the 99% level through related logic packing, this does not mean the device is completely utilized. Unrelated logic packing will then begin, continuing until all usable LUTs and FFs are occupied. Depending on your timing budget, increased levels of unrelated logic packing may adversely affect the overall timing performance of your design.

Timing

Timing errors: 0 Score: 0

Constraints cover 51269 paths, 0 nets, and 18647 connections

Design statistics:

Minimum period: 4.988ns (Maximum frequency: 200.481MHz)

Maximum path delay from/to any node: 4.988ns

From the maximum clock frequency of 200MHz and noting the parallel complex input data format required for a Vectis 'QuadSpeed' core with this configuration, refer to FFT Input Formats, the maximum complex sample rate that can be processed is up to 400MS/s.

Power Requirements

The following figures were generated using the Xilinx Virtex-II Pro Power Estimate Worksheet V1.2.0.

Total Core Power

Target Device	Target Package	Total Estimated Design Power (mW)
XC2VP4	FF672	2218.6667

CLB Logic Power

Name	Frequency (MHz)	Total Number of CLB Slices	Total Number of Flip/Flop or Latches	Total Number of Shift Register LUTs	Total Number of Select RAM LUTs	Average Toggle Rate %	Amount of Routing Used	VCCint Subtotal (mW)
User Module 1	200	3006	5206	696	0	50%	Medium	1124

Block RAM Power

Name	Total Number of BlockRAM Cells	Port A Frequency (MHz)	Port A Width	Port A Read Rate %	Port A Write Rate %	Port B Frequency (MHz)	Port B Width	Port B Read Rate %	Port B Write Rate %	VCCint Subtotal (mW)
User Module 1	12	200	18	0%	100%	200	18	100%	0%	189

**Block Multiplier Power**

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %	VCCint Subtotal (mW)
User Module 1	16	200	Medium	264

Assumptions

Average Toggle rate is set to 50%, as it is assumed that the entire core is run at the clock rate in the above configuration with the 'c_en' input tied to logic '1'. Random data has a 50% toggle rate, and a pessimistic view would be that the whole core is dedicated to the processing of random data.

In addition an assumption is made that all Block RAM elements are 18-bit. In reality some will be less and some will be greater, with wider delays being constructed of several narrow RAM structures in parallel.



ADC	Analogue to Digital Converter
ASIC	Application Specific Integrated Circuit
CLB	Configurable Logic Block
DFT	Discrete Fourier Transform
DHBF	Distributed Half-Band Filter
EDIF	Electronic Data Interchange Format
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
I/O	Input / Output
LSB	Least Significant Bit
MSB	Most Significant Bit
MS/s	Million Samples Per Second
PFT	Pipelined Frequency Transform
PFFT	Pipelined Fast Fourier Transform
RFEL	RF Engines Limited
RTL	Register Transfer Level
RPM	Relationally Placed Macro
UCF	User Constraints File
VHDL	Very High Speed IC Hardware Description Language
VITAL	VHDL Initiative Toward ASIC Libraries

Table 3: Glossary

Please refer to the RFEL web site www.rfel.com for details of PFFT cores under development.

Specifications are subject to change without notice.