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RF Engines Limited



Virtex II Development Board Datasheet

Reference : D02004-Virtex2 Development Board
Revision : 1.3
Date : 31 Oct 2002
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Virtex II Development Board Data Sheet

Introduction

This data sheet describes a board designed by RF Engines Ltd (RFEL) to facilitate the development and testing of cores implemented in Xilinx Virtex II FPGAs. Cores may be purchased from RFEL or produced in-house.

Disclaimer

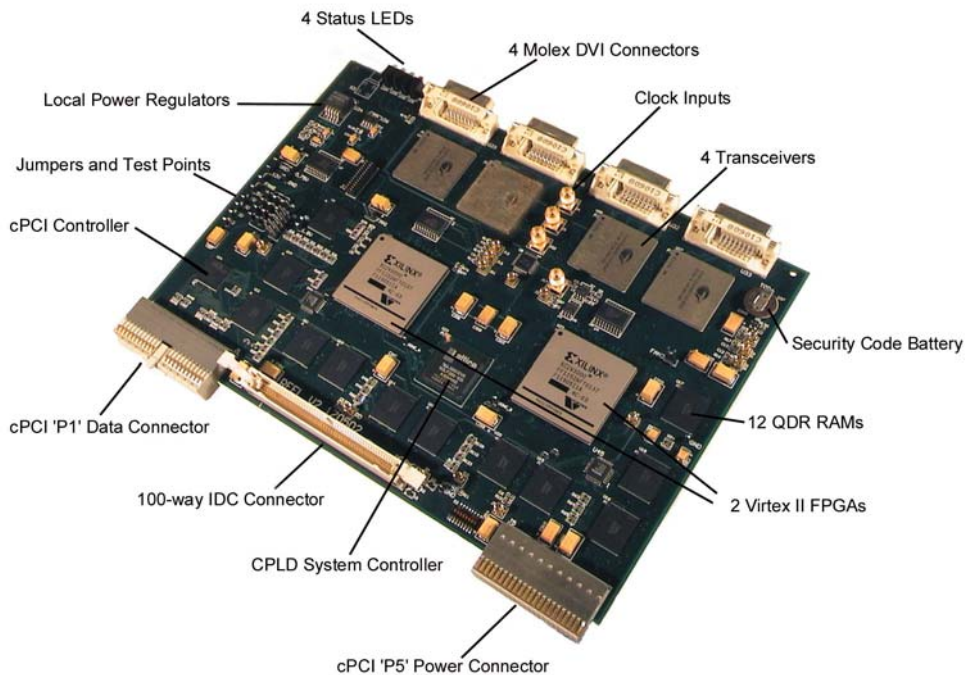
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General Description

The board is sized to fit a 6U cPCI frame, but may be used on the bench if preferred. An associated 6U regulator board providing DC supplies is also available.

Figure 1 – Board Layout



Features

- Two Xilinx Virtex II FPGAs, type XC2V6000 (or 3000,8000,10000).
- Up to a total of 50.4 GMACS performance (18 Bits @ 150MHz for XC2V8000) using dedicated hardware multipliers.
- External Memory resource for **each** Virtex II device :
Six Quad-Data-Rate (QDR) RAMs (Organised in three 36-bit wide banks). Up to 864Mbit total (48M x18) .
One Flash memory. Up to 32Mbit.
- QDR RAM supported:
The board can support either QDR or QDR II RAM. The following devices are supported:
(NOTE: The board can support QDR only or QDR II only, not a mixture of the two. The size of RAM device can be different for each bank if required).

QDR RAM (2.5V core voltage) with XC2V3000
 9Mb 4-word Burst (512k x 18)
 18Mb 4-word Burst (1M x 18)
QDR II RAM (1.8V core voltage) with XC2V3000
 18Mb 4-word Burst (1M x 18)
QDR RAM (2.5V core voltage) with XC2V6000 or larger
 9Mb 4-word Burst (512k x 18)
 18Mb 4-word Burst (1M x 18)
QDR II RAM (1.8V core voltage) with XC2V6000 or larger
 9Mb 4-word Burst (512k x 18)
 18Mb 4-word Burst (1M x 18)
 36Mb 4-word Burst (2M x 18)
 72Mb 4-word Burst (4M x 18)
 144Mb 4-word Burst (8M x 18)
- Flash Memory supported:
Atmel AT45DBxxxB series Flash with 20MHz serial (SPI) interface in the following sizes: 2Mb, 4Mb, 8Mb, 16Mb or 32Mb.
- Aggregate memory bandwidth of 129.6Gbit/s (16.2Gbyte/s) for QDR/QDR II @ 150MHz.
- Theoretical maximum aggregate memory bandwidth of 287.712Gbit/s (35.964Gbyte/s) for QDR II @ 333MHz.
- Each QDR bank can run at a different rate, controlled by the Virtex II.
- Four transceivers, each with a Molex DVI fast serial I/O connector providing 4 input and 4 output lines. An optional board design is available which uses Infiniband 4X connectors.
- Aggregate I/O for board is 19.2Gbits/s input, 19.2Gbits/s output.
- CPLD pre-programmed to control the board set-up and interface control. The CPLD can be user-programmed for alternative set-ups if required via JTAG.

- 100-pin parallel LVTTTL/LVCMOS connector for bench test outputs which provides a 48-bit user definable parallel interface via the CPLD. This interface can be used for data communications with e.g. a microcontroller/USB interface. (Details of a USB 2.0 interface for use with this connector can be supplied by RFEL).
- The board is interfaced to a cPCI bus via a PLX9030 'PCI to Local Bus' controller IC coupled to cPCI connector 'P1'. The PLX9030 allows the board to be interfaced to a 32-bit 33MHz Compact PCI bus and complies with PCI specification V2.2.

The PLX9030 enables an on-board user configurable Local Bus that is routed to the CPLD. The CPLD can be configured as a Local Bus arbiter/controller or can route the Local Bus signals directly to the Virtex II devices for fast data access. Only simple interface logic is required in the Virtex II devices to enable access from the cPCI bus.

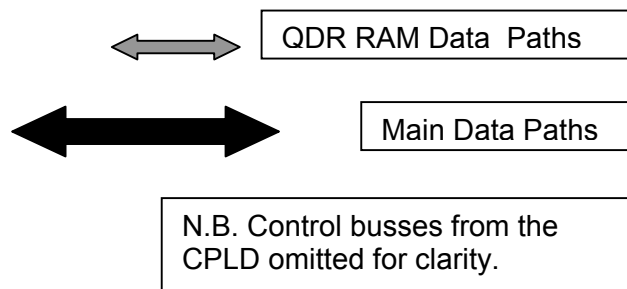
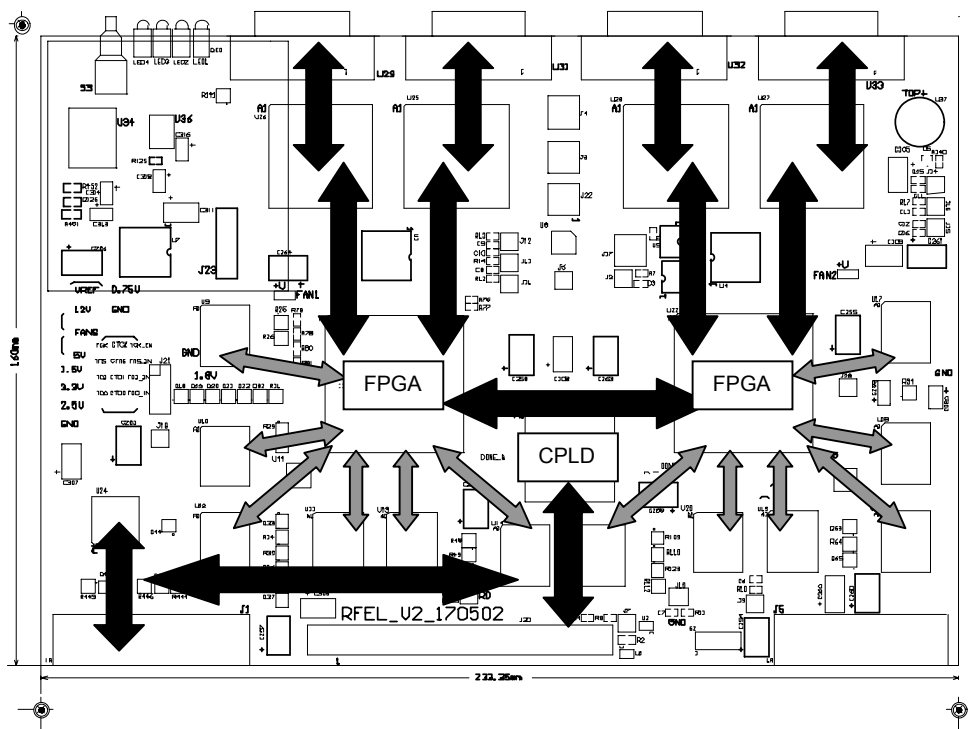
- Minimal loading of the cPCI bus 5V and 3.3V power supplies. The board requires a number of externally generated low voltages that are supplied by a separate voltage regulator board via the 'P5' power supply connector. The regulator board (or board specification) can be supplied by RFEL. Please ask an RFEL sales representative for more information.
- An optional daughter board containing a Xilinx ACE controller and Compact Flash card, providing a choice of FPGA configurations selectable via the built-in 8-way DIL switch *or* via cPCI *or* via the 100-pin microcontroller/USB interface depending on CPLD configuration.
- Option to configure the FPGAs via the JTAG port if the ACE controller daughter board is not used.
- Option to include the cPCI interface in the JTAG chain.
- Front panel providing 4 FPGA status LEDs, 4 Serialiser Link Status LEDs and a manual reset button.
- The board clock input is handled by a PLL device with both programmable frequency synthesis and programmable skew outputs, controlled by the CPLD. The clock input is 3.3V LVTTTL and 5V TTL compatible and can range from 2MHz to 200MHz. The maximum clock supplied to the FPGAs and CPLD is 150MHz, but the FPGAs can synthesize higher frequencies if required. Reference clock frequencies, such as 10MHz, can be supplied to the board with no impact on performance.
- More than 150 I/O lines are routed directly from one Virtex II FPGA to the other. Another 43 lower speed lines can be routed from one FPGA to the other via the CPLD if cPCI/parallel communications are not used.
- Battery backup to retain a configuration security code, if used.
- On-chip temperature monitoring and automatic shut-down of either FPGA.
- On-board connectors for FPGA cooling fans if large, high-speed cores are implemented.

Functional Description

At power-up the FPGAs and CPLD are automatically reset. The behaviour of the board after reset is dependent on the configuration of the CPLD. If the optional SystemACE board is attached, the CPLD can be configured to load one of the eight available FPGA configurations by default. Alternatively, the CPLD can be programmed to wait for an external signal (from the parallel interface, the cPCI local bus or the DIL switch) to load a selected FPGA configuration. The CPLD can also be configured to allow reconfiguration of the FPGA's at any time. Alternatively, the FPGAs can be configured via the JTAG port in which case CPLD is not used to control configuration.

When FPGA configuration is complete, one or both green status LEDs on the front panel will light to confirm a valid configuration. The board will then start to function according to the CPLD and FPGA configurations.

Figure 2 - Functional Block Diagram



Serial I/O

The four quad-transceivers with their Molex DVI (or Infiniband 4X) connectors provide the main high speed I/O facility. These high speed serial ports are each capable of receiving 4 twisted pair inputs to the board and 4 twisted pair outputs from the board. Each twisted pair carries an 8B10B encoded signal running at up to 1.5Gbaud, which results in a true data transmission rate of 1.2Gbits/s. Therefore the total continuous receive capacity into the board is 19.2Gbits/s and transmit capacity is 19.2Gbits/s. The interface to the FPGAs is 8 X 8-bit streams @ 150Mps for each transceiver.

Transceivers can be channel bonded such that each FPGA can transmit/receive 64-bit coherent data at up to 150MHz. (1.2Gbytes/sec per FPGA). Transceivers are Fibre Channel and Gigabit Ethernet compatible and will also work with Xilinx Virtex II Pro Rocket I/O devices.

RFEL Transceiver Board

RFEL have developed a companion transceiver board that can be used to transmit up to 32-bit data e.g. from an A/D converter with a data rate of up to 150Mps, to the Virtex II board and/or receive data from the Virtex II board and output this as parallel data up to 32-bits wide.

The RFEL transceiver boards can be channel bonded from one board to another to allow up to n-bit wide coherent data to be transmitted/received at up to 150MHz, enabling a data interface for (multiplexed) GHz sampling A/D devices. Please contact an RFEL sales representative for details of the RFEL high speed transceiver board.

Parallel I/O

The board supports 48-bits of user defined parallel I/O routed through the CPLD to either/both FPGAs (running at >100MHz) via the 100 way ribbon cable connector. These Parallel I/Os can support a microcontroller/USB interface, or are used for PCI communications for the Local Bus derived from the PLX9030 PCI interface.

IP core support

IP cores can be provided with the following functions:

- QDR RAM Drivers – FIFO, Random Access etc.
- Serialiser Drivers
- PCI interface drivers
- Microcontroller/USB (1.0 or 2.0) Interface drivers
- CPLD pre-defined setups
- CPLD VHDL Wrappers
- FPGA VHDL Wrappers

Software support

The following software can be supplied for use with the board:

- Windows/Linux PCI drivers.
- Windows USB drivers (for an external USB controller).
- A core builder application to link user cores to the provided RFEL drivers for VHDL synthesis.

Please contact an RFEL sales representative for availability of these and other software products.

Third party Software

To get the best performance from the RFEL Virtex II board, the following third party software packages are recommended:

- Mentor Graphics Leonardo Spectrum Level 2 or higher
- Xilinx ISE 5.1 or higher
- Lattice ispLEVER V2.0 or higher

Power Supply Considerations

The current requirements for the 1.5V FPGA supply depends on the size of the configured cores and the clock speed. With the fastest clocks and largest cores in both FPGAs, this figure may be as high as 30A. The 3.3V supply to the FPGA I/O, transceivers and other ICs also depends to some extent on clock rates and will be several Amps.

RFEL have designed a power regulator board which provides 1.5V at 32A from a 3.3V input, and 3.3V at 20A from a 5V input. The regulator board is also sized for a 6U cPCI frame and can be supplied with a supplementary board which links the Virtex II and regulator board P5 connectors on the rear of a cPCI backplane.

Board dimensions

233mm x 180mm x 28mm (without cooling fans fitted).

Applications

While there are many Virtex II board designs in the market place, the RFEL Virtex II development board has primarily been designed for flexibility and very high memory bandwidth. This allows the development of very complex, high speed, 'memory intensive' cores such as those developed in the RFEL core architecture range. Allowing a choice of Virtex II devices (from XC2V3000 to XC2V10000), and a choice of RAM sizes and types means that the board can be tailor-built to both an application and a budget.

The ability of the board to be used in both Rack and 'stand-alone' Bench-top environments means that it is equally well suited to both multi-board, highly intensive signal processing applications, or as a sophisticated piece of Lab equipment, able to execute real-time processing of very high frequency signals.

Application examples

- Communication base station processing
- Multi-channel modulation/demodulation processing
- High-performance IP core evaluation/development

RFEL IP Core Application examples

The following are examples of RFEL IP cores that could run on a single board:

- 4 million point 200Msps Radix-2 Polyphase FFT
- 2 million point 1.5Gsps Radix-8 FFT
- 32k point (15 stage) PFT

More Information

For more information on the RFEL product range please contact an RFEL sales representative or visit the RFEL web site : www.rfel.com

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