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OVERVIEW

This product short-form provides a list of RFEL IP cores that are available for licensing at low cost. Also included are 'off-the-shelf' cores with a detailed listing of their specification parameters. As a result of providing complex, integrated, system design solutions on FPGA, RFEL has developed a number of factory parameterisable, top-level, VHDL designs. These designs are flexible and enable a wide variety of customer specified parameters to be configured by RFEL.

Standard Cores

Standard cores use a part number system to describe their specification. The part number make-up description is contained in the relevant datasheets, which also contain a full list of deliverables.

Design Services

RFEL offers consultancy and integrated design services at cost-effective rates. If you require a subsystem design or a number of our standard cores integrated into a single design, please contact info@rfel.com for more information.

THE FULL RANGE OF RFEL IP CORES

- ◆ **Pipelined FFTs** – fast FFT cores for high sample rate real-time processing
 - ◆ **Polyphase DFTs** – high quality filter bank for real time processing
 - ◆ **Pipelined Frequency Transform (PFT)** – proprietary multi-resolution high quality flexible filter bank
 - ◆ **Tuneable Pipelined Frequency Transform (TPFT)** – proprietary re-configurable filter bank for extracting a multitude of various bandwidth and shape signals from a wideband input. Replaces a set of traditional digital down-converters in multi-channel applications.
 - ◆ **Distributed Half-Band Filters** – Fs/4 up/down convert and decimate function
 - ◆ **Optimised FIR Filters** – highly efficient FIR implementation
 - ◆ **NCO down-converters** – FPGA replacement for standard DDC ASICs
 - ◆ **CORDICs**
 - ◆ **Interleavers and Multiplexers** – interleaves multiple data streams through a single core
 - ◆ **FFT Windowing** – provides a windowing facility for use with standard FFTs
 - ◆ **Power Accumulation** – provides an accumulated spectral power output for selected number of frames of data.
 - ◆ **Format Converters** – convert signed integer values to single precision floating-point and vice versa.
 - ◆ **Bit Reverser** – provides FFT bin re-ordering to produce a normally ordered FFT output
 - ◆ **Input Buffer** – re-orders and re samples data for parallel FFT input
- N.B. bit reversers and input buffers are off-the-shelf options with the *Vectis* and *Ventrix* range of cores

OFF-THE-SHELF CORE DETAILS

1. The Vectis Range of Pipelined FFT Cores

The pipelined FFT is based on a complex input, radix-2 DIF architecture, with two speed-optimised options:

The Vectis 'HiSpeed' (100MS/s sample rate, complex input)

The Vectis 'QuadSpeed' (400MS/s sample rate, complex input)

For these cores the following specification parameters should be supplied:

Product*	Vectis 'HiSpeed' or Vectis 'QuadSpeed'
Radix	Currently only Radix 2 available as off the shelf
Length*	Powers of 2 from 8 through 131072 points. Larger sizes / variable length are available, but currently not as off the shelf options.
Target technology*	'XV2P' = Xilinx Virtex-II PRO, 'AS' = Altera Stratix 'AS2' = Altera Stratix2, XV2' = Xilinx Virtex-II, 'SP3' = Xilinx Spartan3, 'XVE' = Virtex-E, 'AA' = Altera Apex.

Speed grade	Technology specific '6 for example in Virtex-II'. FPGA size is also useful for assessing suitability to accept PFFT core.
Input bit-width	8 to 22 bits. Larger bit widths are available for 'QuadSpeed'.
Twiddle bit-width	10 to 18 bits. Larger bit widths are available for 'QuadSpeed'.
Output bit-width	8 to 32 bits
Precision	<ul style="list-style-type: none"> ◆ 'H' = High Precision (1 bit growth per stage). ◆ 'S' = Single Multiplier (17 bits used at each stage). ◆ 'U' = User Definable (defined prior to order).
Input Buffer	IB = Input buffer included in core, 'IB2X' = 50% overlap input buffer
Bit Reverser	BR = Bit-reverser included in core.

An example of the product part number required for ordering is shown below. It describes a Vectis QuadSpeed PFFT for implementation in Virtex-II Pro technology, -6 speed grade. The size of the transform is 1024-points with input width of 14-bits, twiddle bit width of 18-bits and output bit width of 24-bits. Internal precision is 'High' and Input Buffer and Bit Reversal data re-ordering functions are required.

Vectis-QS-R2-1024-XV2P-6-14-18-24-H-IB-BR.

* If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *.

2. The Ventrrix Range of Polyphase DFT Cores

The polyphase DFT, sometimes referred to as the WOLA (Weighted OverLap and Add) is an efficient method of implementing a uniformly distributed multi-channel filter bank. The architecture consists of a polyphase front-end that performs the weighting, overlapping and addition, followed by a DFT that is usually implemented using an FFT. The polyphase DFT is generally used in applications that demand filters of high quality in terms of stop-band rejection and filter shape.

The RFEL polyphase DFT solution is built from a highly optimised pipelined polyphase front-end core, tightly integrated with a high performance pipelined FFT core. Both of these cores are highly parameterisable to allow the designer to obtain the optimal solution for the application.

They are offered in two speed-optimised options:

The Ventrrix 'HiSpeed' (100MS/s sample rate, complex input)

The Ventrrix 'QuickSpeed1' (200MS/s sample rate, complex input, critical output sample rate)

The Ventrrix 'QuickSpeed2' (200MS/s sample rate, complex input, twice over sampled output sample rate)

For these cores the following specification parameters should be supplied:

Product *	Ventrrix 'HiSpeed', Ventrrix 'QuickSpeed1' or 'QuickSpeed2'
Radix	Currently only Radix 2 available as off the shelf
Length*	Powers of 2 from 8 through 131072 points. Larger sizes / variable length are available, but currently not as off the shelf options.
Target technology*	'XV2P' = Xilinx Virtex-II PRO, 'AS' = Altera Stratix 'AS2' = Altera Stratix2, 'XV2' = Xilinx Virtex-II, 'SP3' = Xilinx Spartan3, 'XVE' = Virtex-E, 'AA' = Altera Apex.
Speed grade	Technology specific '6 for example in Virtex-II'. FPGA size is also useful for assessing suitability to accept the core.
No of polyphase taps	1 to 15, or don't know
Input bit-width	8 to 22 bits. Larger bit widths are available for 'QuadSpeed'.
Twiddle bit-width	10 to 18 bits. Larger bit widths are available for 'QuadSpeed'.
Output bit-width	8 to 32 bits
Precision	<ul style="list-style-type: none"> ◆ 'H' = High Precision (1 bit growth per stage). ◆ 'S' = Single Multiplier (17 bits used at each stage). ◆ U' = User Definable (defined prior to order).
Bit Reverser	BR = Bit-reverser included in core.

Polyphase Coefficients	Fixed in design or externally loadable
Polyphase Coefficient bit-width	12,14,16, or don't know
Approx filter parameters	Please specify: filter type, pass band, transition band and stop band (Presumes RFEL are to design the filter and provide coefficients)

* If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *.

3. The range of Distributed Half-Band Filters

The RFEL Distributed Half-Band filter (DHBF) is intended for use as a high-speed 'up/down-convert and decimate' base-band processor for sampled RF systems. The core provides $f_s/4$ up/down-conversion using an architecture that is extremely efficient in terms of silicon usage. The output from the standard DHBF has linear phase across the $-f_s/4$ to $f_s/4$ bandwidth.

The core can be used as a high performance front-end for application-specific base-band processing or integrated with other RFEL cores. The DHBF architecture also provides an efficient way for more than one ADC data stream to be interleaved at the input to the core.

For these cores the following specification parameters should be supplied:

Product *	DHBF
Target FPGA*	(XVE = Virtex-E, AA = Altera Apex, AS = Altera Stratix, XV2 = Virtex II, XVPRO = Virtex PRO, SP3 = Spartan III)
FPGA part number	Specify manufacturer's part number (if known)
Input format	Real data in '2's compliment' format, or state ADC device
Number of Inputs	Specify number of real data streams to be connected to the core
Input bit width*	8,10,12,14 etc.
Output bit-width	10,12,14 etc. (RFEL can vary bit growth to specification)
Filter order*	If known, or state the transition band frequency range
Filter stop-band attenuation*	65dB, 75dB, 100dB. Others on request.

* If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *.

4. Programmable Windows

The RFEL range of programmable window cores are primarily intended for use for signal pre-conditioning in high sample rate DSP systems and can be provided with fixed or programmable coefficients. The core processes continuous complex data, with no gaps and is ideally suited for interface with the Vectis range of FFTs to provide weighted FFT outputs. Other formats can be easily accommodated but are not off the shelf.

For these cores the following specification parameters should be supplied:

Product*	Window
Length*	Powers of 2 from 8 through 131072 points. Larger sizes are available, but currently not as off the shelf options.
Target technology*	'XV2P' = Xilinx Virtex-II PRO, 'AS' = Altera Stratix 'AS2' = Altera Stratix2, 'XV2' = Xilinx Virtex-II, 'SP3' = Xilinx Spartan3, 'XVE' = Virtex-E, 'AA' = Altera Apex.
Speed grade	Technology specific '6 for example in Virtex-II'. FPGA size is also useful for assessing suitability to accept the core.
Input bit-width	8,10,12,14 etc.
Coefficients bit-width	10 to 18, or don't know
Output bit-width	8,10,12,14 etc.
Coefficient format*	P = Programmable coefficients, F = Fixed coefficients

* If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *.

5. Power Block Accumulator

The RFEL range of Power Block Accumulator cores are primarily intended for use after an FFT in high sample rate DSP systems. They provide I^2+Q^2 conversion to power and block accumulation. The core processes continuous complex data, with no gaps and is ideally suited for interface with the Vectis 'HiSpeed'

range of FFT cores. The core can be supplied with a fixed accumulation stage or a programmable accumulator stage that is controlled via an external interface.

For these cores the following specification parameters should be supplied:

Product*	BACC
Block length*	Powers of 2 from 8 through 131072 points. other sizes are available, but currently not as off the shelf options.
Target technology*	'XV2P' = Xilinx Virtex-II PRO, 'AS' = Altera Stratix 'AS2' = Altera Stratix2, 'XV2' = Xilinx Virtex-II, 'SP3' = Xilinx Spartan3, 'XVE' = Virtex-E, 'AA' = Altera Apex.
Speed grade	Technology specific '6 for example in Virtex-II'. FPGA size is also useful for assessing suitability to accept the core.
Input bit-width	8,10,12,14 etc.
Blocks to accumulate	1 to 255, or don't know
Output bit-width	8,10,12,14 etc.
Programmable*	P = Programmable number of blocks, F = Fixed number of blocks to accumulate.

* If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *.

6. Integer to Single Precision Format Converter

The integer to single precision format converter core provides conversion from up to 64-bit Signed Integer to IEEE-754 32-bit Single Precision Floating Point Format. Conversion of IEEE-754 32-bit Single Precision Floating Point to Signed Integer can easily be provided, but is not off the shelf.

For this cores the following specification parameters should be supplied:

Product*	FC
Target technology*	'XV2P' = Xilinx Virtex-II PRO, 'AS' = Altera Stratix 'AS2' = Altera Stratix2, 'XV2' = Xilinx Virtex-II, 'SP3' = Xilinx Spartan3, 'XVE' = Virtex-E, 'AA' = Altera Apex.
Speed grade	Technology specific '6 for example in Virtex-II'. FPGA size is also useful for assessing suitability to accept the core.
Input bit-width	8 to 64. Only required for Integer input formats.
Input format	IS = Integer to Single, SI = Single to Integer.
Output bit-width	8 to 64. Only required for Integer output formats.

If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *.

7. The range of CORDIC processors

The RFEL CORDIC (Co-Ordinate Rotation Digital Computer) core provides the means to extract magnitude and phase information from an I&Q data stream, or to provide Sine/Cosine conversion of an input angle vector. The CORDIC is available in two modes. Vectoring mode provides Rectangular (Cartesian) to Polar conversion of two input vectors (e.g. I&Q). Rotational mode provides Sine and Cosine conversion of an input vector, thus providing an accurate quadrature oscillator when coupled with a ramp generator.

The accuracy of the output is determined by the internal arithmetic bit-width and the number of iterations (clock cycles) the processor takes to produce an output. These parameters can be specified by the customer or optimised by RFEL to meet accuracy specifications. The CORDIC processor is available in two distinct architectures: 'Iterative' for low speed, high silicon efficiency solutions, and 'Pipelined' for high speed applications. The main features are listed below, with speeds based on Xilinx Virtex-II or Altera Stratix FPGAs:

Architecture	Features
Iterative Vectoring	Low silicon usage. Max data output rate better than (100MS/s/Number of iterations)
Iterative Rotational	Low silicon usage. Max data output rate better than (100MS/s/Number of iterations)
Pipelined Vectoring	Optimised for speed. Data throughput better than 200MS/s
Pipelined Rotational	Optimised for speed. Data throughput better than 200MS/s

For these cores the following specification parameters should be supplied:

Product *	CORDIC
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Mode*	Vectoring or rotational
Architecture*	Iterative or pipelined
Target FPGA*	(XVE = Virtex-E, AA = Altera Apex, AS = Altera Stratix, XV2 = Virtex-II, XVPRO = Virtex-II PRO, SP3 = Spartan III)
FPGA part number	Specify manufacturer's part number (if known)
Input bit-width	8,10,12,14 etc.
Delivery format	Netlist or Bitstream
Max input sample rate (fs)*	XXX MS/s
Vectoring mode magnitude resolution (bit-width)	Specify number of bits, or resolution
Vectoring mode phase resolution (bit-width)	Specify number of bits or phase-angle resolution
Rotational mode output bit-width	Specify number of bits
Number of iterations	If known, otherwise this will be calculated from resolution specification.
CORDIC gain compensation*	Yes/No

* If all the information required is not readily available in the first instance, RFEL can provide a budgetary quotation from the parameters indicated by a *

PRICING, DELIVERY AND QUOTATIONS

The designs are provided in netlist or bitstream form on a per-use licence basis. A single use licence can be purchased for prototype designs and then upgraded to a higher number of uses at a later date. Standard price breaks are set at 1,10, 50 and 100 uses. Quantities above 100 uses are negotiated on an individual basis.

The prices for standard cores assume that the design will fit comfortably into the chosen FPGA and it is a single FPGA solution. For designs that require two or more FPGAs there will be a nominal non-recurring engineering charge to produce the cores. Prices start from \$1500. Please note there will be an additional NRE charge if RFEL is required to design the polyphase filter coefficients for the fixed design *Ventrix* range. All deliveries will be by electronic transfer.

To obtain a quotation for your chosen core please send an email to info@rfel.com with the part number derived from the information above.

MODEL AVAILABILITY

RFEL can provide a range of Matlab and SystemView models. The models are in floating point and bit-true formats. They allow various parameters to be selected so that exact replication of the hardware performance can be simulated.

Off-the-shelf parameterisable models are currently available for :

The *Vectis* range of Pipelined FFT cores
The *Ventrix* range of Polyphase DFT cores
The Pipelined Frequency Transform (PFT)

Models can also be provided to order for :

The Tuneable Pipelined Frequency Transform (stand alone .exe model)
The range of DHBFs, and the other cores listed above.

PRODUCTS IN DEVELOPMENT

The *Vectis* 'HyperSpeed' FFT cores – this is a specialist range of FFT cores designed to work with effective ADC sample rates up to 4GS/s.

The *Matrix* range of mixed radix FFT cores – a range of FFT cores designed to perform FFTs of any length.

The *Vortex* range of multi-rate filter cores – a highly efficient structure for filtering and/or rate conversion.

Due to ongoing product development and enhancements, RF Engines reserves the right to alter specifications without notice