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Product Specification and User Guide - SpectraChip Digital IF Spectrum Analyser FPGA Core

PART NUMBER
SpectraChip –Digital IF –XV2 -001

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OVERVIEW

This document describes the RF Engines Ltd (RFEL) SpectraChip Digital IF for Spectrum Analyser FPGA core. This core is intended as a replacement for the conventional analog IF module in swept spectrum analysers and provides all of the standard functions including resolution bandwidth (RBW) control, I & Q to power conversion, video bandwidth (VBW) control and floating point output conversion. A fixed 30 kHz flat output band is also included for narrowband FFT display. The core is supplied in EDIF netlist form as a component.

CORE VERSION

1.0

DELIVERABLES

Supplied Item	Description
Design	EDIF netlist
Constraints File	UCF (User Constraints File)
Instantiation Template	VHDL
Verification	VHDL test bench including ModelSim script and test data files. Compiled RTL VHDL Model. Bit-true Matlab model and scripts. Placement reports.

Table 1: Items provided with each core

GENERAL DESCRIPTION

The basic architecture of the core is shown in Figure 1 below. This particular core is designed to accept a 14 bit output from the ADC using an IF of 21.4 MHz and a sampling frequency of 64.2 MS/s. Other IF's and sampling rates are available in the SpectraChip range. The digital down-converter (DDC) block converts the real input sample stream to a complex I &Q baseband at 21.4 MS/s with up to 15 bits output. The next block is a 5 stage CIC with variable integer decimation from N=1 to 150,000. Both the input gain and CIC decimation are user-controlled parameters.

To provide full backwards compatibility with standard spectrum analyser practice, the next block is a 16 tap, decimate-by-1 or 32 tap, decimate-by-two FIR filter. This, combined with the 5-stage CIC, provides a Gaussian shaped resolution bandwidth (RBW) filter with RBW values in the range 10 Hz to 3 MHz. The coefficients may be user defined to give a wide choice of RBW values or chosen from a pre-calculated set giving a 1 : 3 : 10 RBW ratio over the above range. Once corrections for CIC and any analog filter roll-off have been accounted for, the RBW accuracy can be held well within ±5% with shape factors (-60dB to -3dB) of better than 5:1.

The 'Complex to Power' block simply performs an I^2+Q^2 function on the complex data. The video filter is also capable of giving a wide range of video bandwidth (VBW) values between 1 Hz and 1MHz with pre-calculated settings for 1Hz, 10Hz, 100Hz etc. thro' 1MHz. In this case, the VBW is defined as the 'equivalent noise bandwidth' (ENB) rather than the 3 dB bandwidth (although the values will be similar).

One additional output is designed to give the user the option of performing a narrowband FFT, external to the FPGA core (normally using a programmable DSP). This is especially useful for speeding up the narrowest RBW measurement, compared with the conventional swept mode. Thus, for example, providing a flat filtered output over a 30 kHz span and an external 1K complex FFT with Gaussian weighting would allow an RBW of typically 50Hz to 100 Hz to be formed. The settings and weighting functions for this are available as pre-calculated parameters and the user can calculate additional parameters as required.

To give maximum flexibility and to aid system de-bugging, a wide range of outputs may be selected via the Output Select control line. Essentially, the user may select the output from any major functional block from the ADC data through to the video filtered power, as shown in Figure 1 below.

When using high decimation factors (for narrow RBW's) the bit-growth required to maintain the available dynamic range can be very large (typically close to 60 bits for the PWR modes) which, in turn, would lead to a very wide interface data bit-width. The preferred method, therefore, is to convert to a standard 32 bit floating point value. A 'fixed to floating' point conversion block is provided for this purpose after the 'output select' block.

Finally, some degree of buffering at the data output will be required, even where high continuous data rates can be maintained by the receiver. The amount of available 'on-chip' FIFO will very much depend on the specific FPGA and the amount of FIFO essential for continuous data transfer will depend on the received data rate that can be supported.

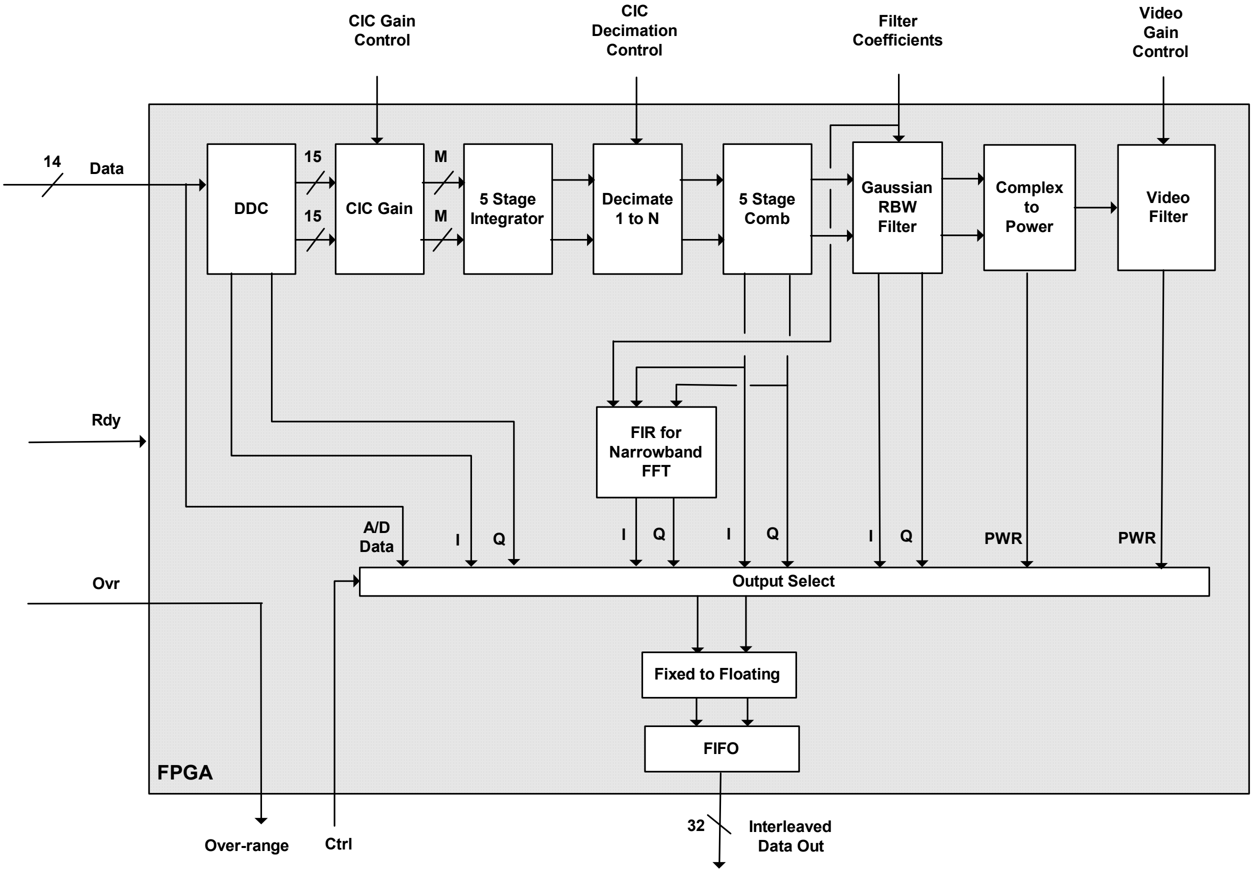


Figure 1: SpectraChip Functional Block Diagram

RESOLUTION BANDWIDTH (RBW) FILTER PARAMETERS

General Description

The RBW filters, as described above, require an approximate Gaussian shape and are formed from a 5-stage CIC filters cascaded with a 16 tap, non-decimating or a 32 tap decimate-by-two FIR filter. This arrangement gives a good approximation to Gaussian with a shape factor of, typically, 4.5:1 (exact Gaussian is 4.47:1). Some alias sidelobes are present but these will always be below the quantisation and/or system noise level for the given RBW and full-scale input and should not, therefore, appear as a display artifact. An illustration for the case of RBW = 300 kHz and a span of 9 MHz is shown in Figure 2 below.

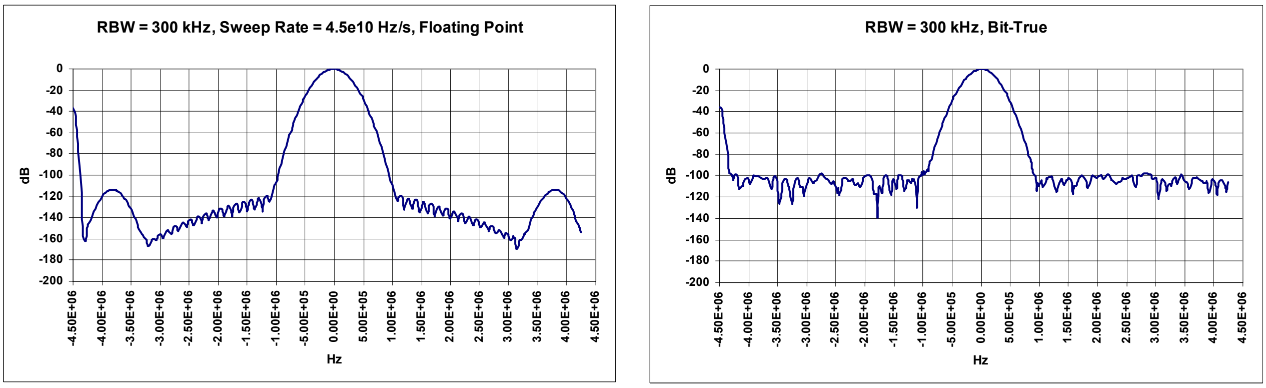


Figure 2: Comparison of Floating Point & Fixed Point Simulations for RBW = 300kHz

In this particular case, the underlying floating-point filter design would have frequency alias sidelobes at ±3.8 MHz offset (approx. ±12.7xRBW) at a level of –114 dBc. When quantisation noise is taken into account in the bit-true results, it is seen that the noise floor obscures these alias sidelobes. A further effect, which should be taken into account, is that of the analog pre-filter. It is normal, in real systems, to use an analog pre-filter to maximise the dynamic range. This will typically have 3 to 5 times the bandwidth of the RBW filter and is a compromise between having minimal effect on the RBW filter response whilst reducing the effects of large signals close to the signal being measured. These filters will, typically, be Gaussian or Bessel to minimise transient response effects and a typical effect of a 900 kHz Bessel pre-filter on the underlying 300 kHz RBW is shown in Figure 3 below.

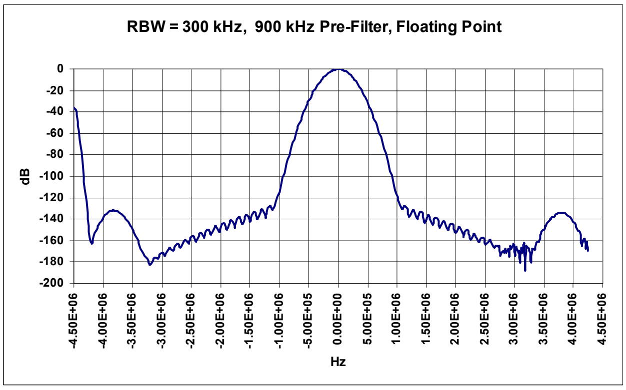


Figure 3: Effect of 900 kHz Bessel Pre-Filter on Underlying Sidelobes for RBW = 300 kHz

It can be seen that the underlying sidelobes have been reduced from –114 dBc to –132 dBc which is even further below the quantisation noise level. This effect cannot be relied upon at the narrower resolution bandwidths, however, because there will be a practical limit to the minimum pre-filter bandwidth of, typically, 3 to 5 kHz. Table 2 below gives typical worst case alias sidelobes for different RBW's using 1-pole Bessel pre-filters.

RBW (Hz)	1-Pole Bessel Pre-Filter B/W (Hz)	Quantisation Noise (dBc)	Worst Alias Sidelobe (No Pre-Filt) (dBc)	Worst Alias Sidelobe (Pre-Filt) (dBc)	Offset Frequ (Hz)
3.00E+06	None	-90	None	None	-
3.00E+05	9.00E+05	-100	-114	-132	3.80E+06
3.00E+04	9.00E+04	-110	-117	-135	3.80E+05
3.00E+03	9.00E+03	-120	-117	-135	3.80E+04
300	5.00E+03	-130	-117	-126	3.80E+03
30	5.00E+03	-140	-117	-121	3.80E+02
10	5.00E+03	-145	-117	-121	1.30E+02

Table 2: Effect of Typical Pre-Filters on Frequency Sidelobes

It will be noted that, in this example, for RBW's of 300 Hz or less, the alias sidelobe can be seen above the quantisation noise. However, because these sidelobes are quite close to centre frequency, they will normally be obscured by the effect of oscillator phase noise. Taking the example of 300 Hz RBW, the worst sidelobe is at 3.8 kHz offset at a level of –126 dBc/ 300 Hz which equates to –150.8 dBc / Hz. This level is well below the likely phase noise at this offset for typical spectrum analysers. By the same argument, the lower RBW's present even less of a problem.

The whole objective of the RFEL core design has been to minimise silicon whilst giving excellent filter performance. It should be noted that system thermal noise has not been included since this is dependent on the RF section design. System noise will further obscure any residual effects of alias sidelobes.

It is important to note that the above limitations *are not fundamental* and that improved filters can be easily designed at the expense of slightly increased silicon (*contact RFEL to discuss special requirements*)

RBW Specifications

The specifications for the standard RBW values for this core are shown in Table 3 below. This is based on the conventional 1 : 3 : 10 sequence adopted by most spectrum analyser designs, over the range of RBW values from 3 MHz to 10 Hz.

Once again, it is stressed that these limitations *are not fundamental* and that much finer steps in RBW are available. Similarly, extensions to both minimum and maximum RBW are available although the latter may require a change of sample rate (*contact RFEL to discuss special requirements*).

Parameter	Specification			
FPGA Type	Xilinx Virtex II 1000			
Input data bit width and format	14 Bits real, Signed Integer			
Input data clock rate	64.2 MS/s			
Input signal IF	21.4 MHz			
	RBW	Form Factor[1]	Dynamic Range[2]	RBW Accuracy
	3 MHz	4.0 Min. 4.7 Max	75 dBc	+/- 5%
	1 MHz	4.0 Min. 4.7 Max	80 dBc	+/- 5%
	300 kHz	4.0 Min. 4.7 Max	85 dBc	+/- 5%
	100 kHz	4.0 Min. 4.7 Max	90 dBc	+/- 5%
	30 kHz	4.0 Min. 4.7 Max	95 dBc	+/- 5%
	10 kHz	4.0 Min. 4.7 Max	100 dBc	+/- 5%
	3 kHz	4.0 Min. 4.7 Max	105 dBc	+/- 5%
	1 kHz	4.0 Min. 4.7 Max	110 dBc	+/- 5%
	300 Hz	4.0 Min. 4.7 Max	115 dBc	+/- 5%
	100 Hz	4.0 Min. 4.7 Max	120 dBc	+/- 5%
	30 Hz	4.0 Min. 4.7 Max	125 dBc	+/- 5%
	10 Hz	4.0 Min. 4.7 Max	130 dBc	+/- 5%
RBW definition point	-3dBc point			

Table 3: Standard RBW Specifications

Table 3 Notes:

1. Definition of Form Factor

Ratio of –60dB bandwidth to –3dB bandwidth

2. Definition of Dynamic range

Centre of filter response to worst side-lobe.

COMPLEX I & Q TO POWER CONVERSION

Immediately following the output from the CIC & Gaussian filter stage, a complex to power conversion is carried out, as shown in Figure 1. Since no phase information is required, a straightforward $I^2 + Q^2$ operation is used. The important point is to maintain adequate dynamic range to which end, this core supports 29 bits complex input and 58 bits real output

VIDEO BANDWIDTH (RBW) FILTER PARAMETERS

General Description

This core uses a highly efficient form of video filtering, based on CIC filters, which gives 'close-to – Gaussian' filter characteristics. Unlike the RBW filters, the shape factor and alias sidelobe levels are less critical, the transient response and equivalent noise bandwidth (ENB) being more important parameters. The design aim has been to ensure low transient overshoot (as per Gaussian characteristics), with better than –50 dBc frequency sidelobes and ENB within ± 5% of design value.

Figure 4 below shows the effect of a 10 kHz VBW filter over a 9 MHz span using a 300 kHz RBW. The sweep speed has been slowed from the usual 4.5e10 Hz/s (i.e. $0.5*RBW^2$) to 1.5e9 Hz/s (i.e. 0.5*RBW*VBW) to allow for the narrow VBW filter bandwidth.

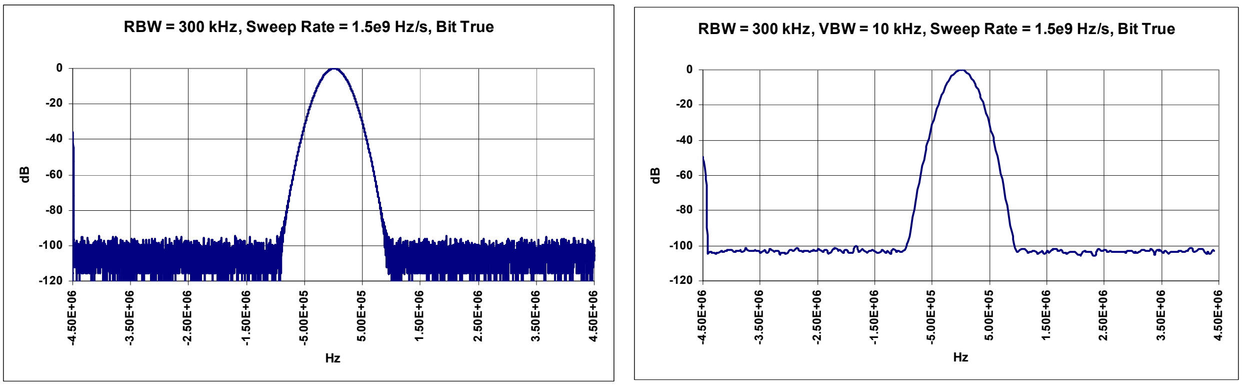


Figure 4: Comparison of 300 kHz RBW, With & Without 10 kHz VBW, Span = 9 MHz, Sweep Rate = 1.5e9 Hz/s

VBW Filter Specifications

Table 4 below shows the range of valid combinations of RBW and VBW. One absolute requirement is that the VBW will always be less than or equal to the RBW value. A second limitation, based on the maximum CIC bitwidth of 116 bits, is that the combinations marked with an 'x' are not realisable. Again, it is stressed that this limitation *is not fundamental* and that these combinations *could* be realised at the expense of more silicon.

The second thing that Table 4 shows is the actual measured equivalent noise bandwidth (ENB) for the various combinations. The typical value is between 2% and 3% above nominal value but for the specific cases where RBW and VBW are equal, the error rises to +8.2%.

To maintain internal precision, the VBW CIC filter bitwidth of up to 128 bits is allowed although, as mentioned above, only 116 bits is used in order to maintain the required clock rates through the CIC adder chains.

	Measured Equivalent Noise Bandwidth (ENB) - Hz						
RBW (Hz)	**VBW 1.00E+06 (Hz)**	**VBW 1.00E+05 (Hz)**	**VBW 1.00E+04 (Hz)**	**VBW 1.00E+03 (Hz)**	**VBW 100 (Hz)**	**VBW 10 (Hz)**	**VBW 1 (Hz)**
3.00E+06	1.029E+06	1.023E+05	1.023E+04	1.023E+03	x	x	x
1.00E+06	1.082E+06	1.024E+05	1.023E+04	1.023E+03	x	x	x
3.00E+05		1.029E+05	1.023E+04	1.023E+03	102.3	x	x
1.00E+05		1.082E+05	1.024E+04	1.023E+03	102.3	x	x
3.00E+04			1.029E+04	1.023E+03	102.3	10.23	x
1.00E+04			1.082E+04	1.024E+03	102.3	10.23	x
3.00E+03				1.029E+03	102.3	10.23	1.023
1.00E+03				1.082E+03	102.4	10.23	1.023
300					102.9	10.23	1.023
100					108.2	10.24	1.023
30						10.29	1.023
10						10.82	1.024

Table 4: Valid Combinations of RBW and VBW & Measured ENB Values

NARROWBAND FFT FIR FILTER OUTPUT

An output is provided which selects a 30 kHz filtered complex (I & Q) output. This allows an FFT to be performed, external to the core (typically in a programmable DSP), thus potentially speeding up spectral analysis for narrow RBW's. For this mode, the spectrum analyser local oscillators must be at fixed frequencies (i.e. zero span mode). The sample rate for this output (and for this particular core) is only 37.412 kS/s, complex which may easily be achieved in real-time using a programmable DSP.

The narrowband output is formed by cascading a FIR with 127 Taps and decimation factor of 4 and the CIC which is set to a decimation factor of 143. The overall decimation factor of 572 from the input sample rate of 21.4 MS/s provides the output rate of 37.142 kS/s. It is also necessary to compensate for the 5-stage CIC roll-off, which gives around 0.8 dB droop in the ±15 kHz passband. This is done by pre-compensating the 127 Tap FIR weights, which yields a droop of less than 0.015 dB together with a ripple of less than ±0.01 dB in the passband. With the coefficients set to 18 Bits quantisation, a stop-band level of better than –100 dBc is achieved. Figure 5 and Figure 6 below show the measured filter response in relative (dBc) form.

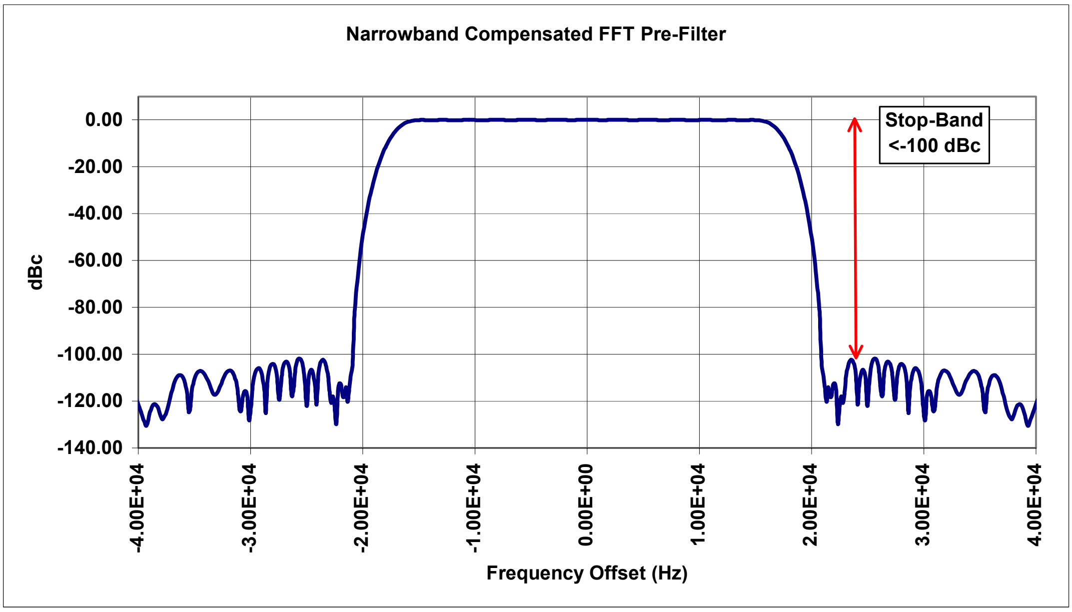


Figure 5: Overall Response of Narrowband Compensated FFT Pre-Filter

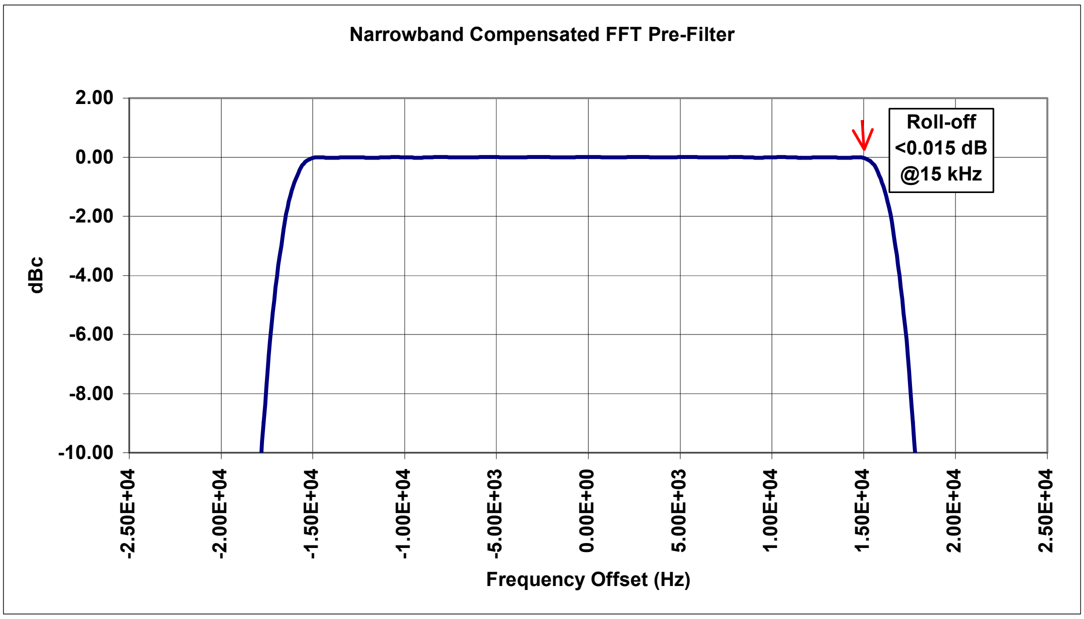


Figure 6: Passband Detail of Figure 5 Showing Compensated Roll-Off

OUTPUT SELECT

To give maximum flexibility to the core and to allow some degree of hardware de-bugging, an output select MUX is included which can select any of the outputs of Table 5 below.

Selected Output	Format	Precision
A to D Converter	Real	14 Bit, Converted to 32 Bit Floating Point, Non-Interleaved
Digital Downconverter	Complex (I & Q)	15 Bit Complex, Converted to 32 Bit Floating Point, Interleaved
Narrowband FFT FIR Output	Complex (I & Q)	32 Bit Complex, Converted to 32 Bit Floating Point, Interleaved
RBW CIC Filter Output	Complex (I & Q)	32 Bit Complex, Converted to 32 Bit Floating Point, Interleaved
Gaussian RBW Filter Output	Complex (I & Q)	29 Bit Complex, Converted to 32 Bit Floating Point, Interleaved
Output of Complex to Power Converter	Real	64 Bit, Converted to 32 Bit Floating Point, Non-Interleaved
Video Filter Output	Real	64 Bit, Converted to 32 Bit Floating Point, Non-Interleaved

Table 5: Selectable Core Outputs

The first, second and fourth selectable outputs are, primarily, provided as a de-bugging aid. However, the Digital Downconverter does provide a flat 10 MHz passband which could be useful for wideband analysis provided a sample rate of 21.4 MS/s (complex) can be maintained *or* provided the output FIFO size is adequate (see below). *Note that RFEL also provides cores with wideband real-time capability – contact RFEL for details.* Similarly, the CIC output could also be useful for constructing different shaped filters (using polyphase decimating FIR techniques external to the core).

The narrowband FFT FIR output has been described in the 'Narrowband FFT FIR filter output' section above.

The complex output from the Gaussian filter is made available so that alternative external processing, requiring phase and amplitude information (for example, zero span signal demodulation) may be carried out.

The two final selectable outputs represent the power of the swept signal both with and without video filtering.

FIXED TO FLOATING POINT CONVERSION

The bit-widths of the final outputs of this core can be very wide. Because of the high decimation factors and narrow final RBW values this core requires up to 29 bits I & Q output or 58 bits for power. For this reason, the data output is converted to a single output, 32 bit floating point (IEEE-754) format. In the case of complex (I & Q) data, the data streams are interleaved at the output as shown in Table 5 above.

OUTPUT FIFO

A brief mention of the need for an output FIFO is necessary although it *does not actually form part of the Core itself.* The need for this will be driven by the users application and the buffer size will depend on the highest sustainable data transfer rate. The data will be written to the FIFO synchronously with the core clock and because of the likelihood that the output will be read asynchronously under DSP control, some degree of buffering will always be necessary. In the case where the highest data rate (for this core) of 21.4 MS/s, complex, cannot be maintained continuously, then enough buffer must be provided to contain at least one scan of data. The time of this will depend on the user's application (sweep speed, span etc.) but, as a guide, RFEL have found that a minimum buffer size of 16 Kbytes is needed

INTERNAL PRECISION AND SCALING

The internal arithmetic precision of the core is shown in Table 6 below, where ‘Bit-width’ defines the number of signed 2’s-complement bits used for each of the data path outputs from each stage (except the Float Converter which is 32 bit floating point).

Stage	Output Bit-width	Real / Complex
Input	14	Real
DDC	15	Complex
CIC	116 (internal)	Complex
Gaussian FIR	29	Complex
Narrow FFT FIR	54	Complex
Power	58	Real
Video Filter	64	Real
Select MUX	64	Real / Complex
Float Converter	32	Real / Complex

Table 6: Internal Precision

Once again, it is stressed that *these are not fundamental limitations* and that customised bit-widths can be provided (*contact RFEL to discuss special requirements*).

LATENCY

Latency is defined as the time from when the first input sample is clocked into the Core to the time when the first valid output sample (real or complex) is clocked out from the core. With a core such as this with multiple outputs, multiple control parameters and some recycling in the architecture, the measurement of latency is not simple. Furthermore, the latency as defined here should not be confused with group delay which is caused by the various filter elements in the system, both digital and analog. Some guidance on the subject of group delay is given in the following section.

In order to simplify the problem of predicting exact latency (excluding group delay) for each combination of settings, a synchronisation pulse is provided which indicates first valid sample out.

GROUP DELAY

As discussed above, there are additional delays in the system due to both analog and digital filters. The discussion here is restricted to the digital filters implemented in this core but the system designer is reminded that analog filter delays will need to be accounted for in order to perform accurate swept spectrum analysis measurement.

The group delays for this core are shown in Table 7 below and include the delay for the narrowband FFT FIR but exclude the effects of the VBW filters, when used. The additional video filter group delay may be calculated from the following expression:-

$$\text{VBW Group Delay} = 0.5*(15R+5)/F_{in}$$

Where: R = VBW CIC Decimation

F_{in} = VBW CIC Input Sample Rate

= RBW Filter Output Sample Rate

As an example, if we take RBW = 300 kHz and VBW = 10 kHz, from Table 7 below, the RBW output sample rate is 2.14e6 Hz. Also, from Table 9 below, R = 30 which, using the above expression, gives a value:

$$\text{VBW Group Delay} = 0.5*(15*30+5)/2.14e6 \text{ (s)}$$

$$= 106.31 \text{ uS}$$

RBW	CIC Input Sample Rate (Hz)	CIC Decimation	DDC Delay (s)	CIC Delay (s)	16 Tap Gaussian Delay (s)	32 Tap Gaussian Delay (s)	FIR Decim	Total Group Delay (s)	Output Sample Rate (Hz)	No. of Samples Delay
3.00E+06	2.14E+07	1	2.49221E-07	2.33645E-07	3.50E-07		1	**8.33E-07**	2.14E+07	17.83
1.00E+06	2.14E+07	3	2.49221E-07	4.6729E-07	1.05E-06		1	**1.77E-06**	7.13E+06	12.61
3.00E+05	2.14E+07	5	2.49221E-07	7.00935E-07		3.62E-06	2	**4.57E-06**	2.14E+06	9.78
1.00E+05	2.14E+07	15	2.49221E-07	1.86916E-06		1.09E-05	2	**1.30E-05**	7.13E+05	9.26
3.00E+04	2.14E+07	50	2.49221E-07	5.95794E-06		3.62E-05	2	**4.24E-05**	2.14E+05	9.08
1.00E+04	2.14E+07	150	2.49221E-07	1.76402E-05		1.09E-04	2	**1.27E-04**	7.13E+04	9.03
3.00E+03	2.14E+07	500	2.49221E-07	5.8528E-05		3.62E-04	2	**4.21E-04**	2.14E+04	9.01
1.00E+03	2.14E+07	1500	2.49221E-07	0.00017535		1.09E-03	2	**1.26E-03**	7.13E+03	9.00
3.00E+02	2.14E+07	5000	2.49221E-07	0.000584229		3.62E-03	2	**4.21E-03**	2.14E+03	9.00
1.00E+02	2.14E+07	15000	2.49221E-07	0.001752453		1.09E-02	2	**1.26E-02**	7.13E+02	9.00
3.00E+01	2.14E+07	50000	2.49221E-07	0.005841238		3.62E-02	2	**4.21E-02**	2.14E+02	9.00
1.00E+01	2.14E+07	150000	2.49221E-07	0.017523481		1.09E-01	2	**1.26E-01**	7.13E+01	9.00
30 kHz FFT										
FIR	2.14E+07	143	2.49221E-07	1.68224E-05		4.21E-04	4	**4.38E-04**	3.74E+04	16.39
						*NB 127T FIR				

Table 7: Filter Group Delays for SpectraChip Core, 64.2 MS/s Version

PHYSICAL COMPONENT INTERFACE INFORMATION

Component Port Definitions

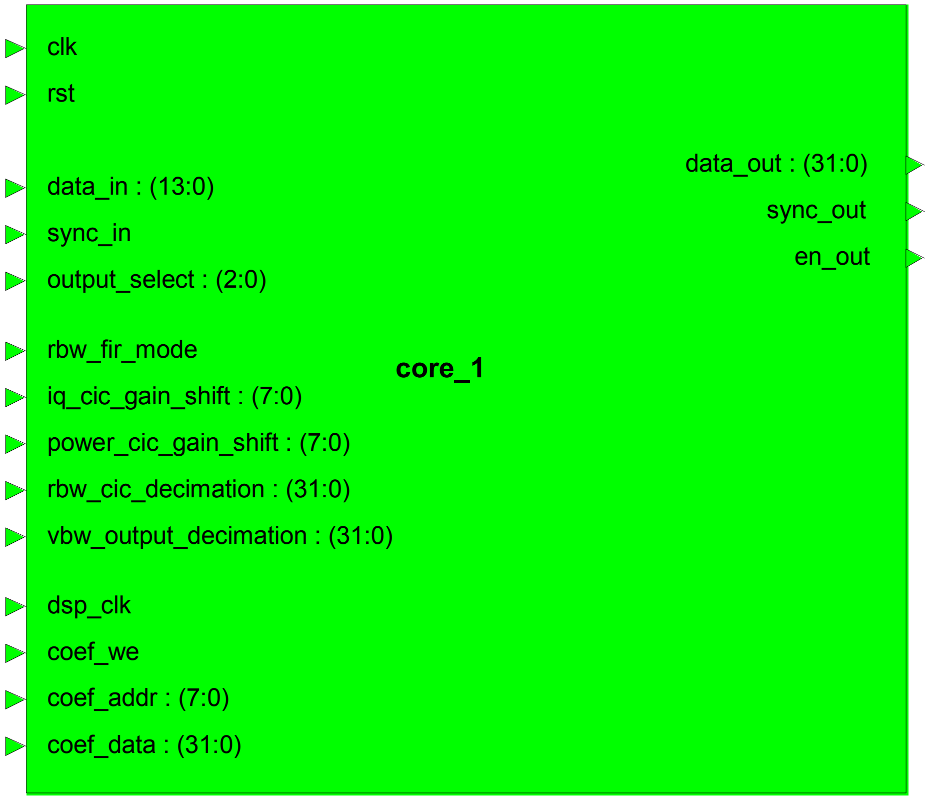
Component Diagram

Package List
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;

Declarations
Ports:

```
    clk                   : IN     STD_LOGIC  ;
    rst                   : IN     STD_LOGIC  ;
    sync_in               : IN     STD_LOGIC  ;
    rbw_fir_mode          : IN     STD_LOGIC  ;
    iq_cic_gain_shift     : IN     STD_LOGIC_VECTOR (7 downto 0) ;
    power_cic_gain_shift  : IN     STD_LOGIC_VECTOR (7 downto 0) ;
    rbw_cic_decimation    : IN     STD_LOGIC_VECTOR (31 downto 0) ;
    vbw_output_decimation : IN     STD_LOGIC_VECTOR (31 downto 0) ;
    dsp_clk               : IN     STD_LOGIC  ;
    coef_we               : IN     STD_LOGIC  ;
    coef_addr             : IN     STD_LOGIC_VECTOR (7 downto 0) ;
    coef_data             : IN     STD_LOGIC_VECTOR (31 downto 0) ;
    output_select         : IN     STD_LOGIC_VECTOR (2 downto 0) ;
    data_in               : IN     STD_LOGIC_VECTOR (13 downto 0) ;
    data_out              : OUT    STD_LOGIC_VECTOR (31 downto 0) ;
    en_out                : OUT    STD_LOGIC  ;
    sync_out              : OUT    STD_LOGIC
```

User:



Component Interface Table

Group	Mode	Name	Size	Description
Global	IN	clk	1	Global clock used by this block. **Must be 64.2MHz**.
Global	IN	rst	1	Global reset of all control logic. But no effect on data path logic. Active High.
Input	IN	data_in	13:0	Data from the ADC
Control	IN	sync_in	1	Re-syncs control to identify I sample. Can be tied to 0v. Active High.
Control	IN	output_select	2:0	Selects 1 of 8 outputs 0 = ADC Data 1 = D3BF (DDC) Data 2 = RBW CIC I/Q (interleaved) 3 = Pre-S/W FFT filter output 4 = RBW Power 5 = RBW I/Q (interleaved) 6 = VBW Power 7 = Not Used
Control	IN	rbw_fir_mode	1	Fixed control input per mode of operation. 0=16 tap RBW FIR 1=32 tap RBW FIR
Control	IN	iq_cic_gain_shift	7:0	RBW Gain shift. Fixed control input per mode of operation.
Control	IN	power_cic_gain_shift	7:0	VBW Gain shift. Fixed control input per mode of operation.
Control	IN	rbw_cic_decimation	31:0	RBW Decimation. Fixed control input per mode of operation
Control	IN	vbw_output_decimation	31:0	VBW Decimation. Fixed control input per mode of operation
Control	IN	dsp_clk	1	Clock used to write to dual port ram, containing 32 RBW Filter Coefficients.
Control	IN	coef_we	1	Write Enable used to write to dual port ram, containing 32 RBW Filter Coefficients. Active High.
Control	IN	coef_addr	7:0	Address used to write to dual port ram, containing 32 RBW Filter Coefficients.
Control	IN	coef_data	31:0	Data written to dual port ram, containing 32 RBW Filter Coefficients.
Output	OUT	data_out	31:0	Floating point (IEEE-754) Data Output after signal processing.
Control	OUT	sync_out	1	Valid I sample or power sample output. Active High
Control	OUT	en_out	1	Valid sample output. Active High

Component Interface Detailed Descriptions

clk:

Global clock used by the RFEL FPGA Core must be 64.2MHz. This can be taken from the RDY signal of the ADC.

rst:

This is an active high control signal, used to reset the control logic, but has no effect on data path logic.

This control signal should be pulsed at the end of each mode change (after the set up of control registers and loading of coefficients), to latch in the new control data and restart the cores timing and control logic.

This should be at least four 64.2 MHz clock period long.

data_in:

This is the 14 bit data straight from the ADC.

sync_in:

This is an optional active high control input. By pulsing it for one 64.2 MHz clock period will reset the phase (identify the I sample present at the input of the core) of the third band filter.

This can be tied to ground if this phase control is not required.

output_select:

This control signal bus is used to select 1 of 8 outputs presented on the output ports of the core.

0 = ADC Data

1 = D3BF (DDC) Data

2 = RBW CIC I/Q (interleaved)

3 = Pre-S/W FFT filter output

4 = RBW Power

5 = RBW I/Q (interleaved)

6 = VBW Power

7 = Not Used

This control signal bus is static for each mode of use and should be held stable whilst the rst signal is high, when it will be latched into the core.

rbw_fir_mode:

This control signal bus is used to set the mode of the Resolution Bandwidth FIR filter.

0=16 tap RBW FIR

1=32 tap RBW FIR

The appropriate filter coefficient values for each mode of operation are defined in Table 8 and Appendix B – List of Pre-calculated filters.

This control signal bus is static for each mode of use and should be held stable whilst the rst signal is high, when it will be latched into the core.

iq_cic_gain_shift:

This control signal bus is used to set the data shift at the inputs to the Resolution Bandwidth CIC filter.

The appropriate values for each mode of operation are defined in the 'Control Signal Information' section below

This control signal bus is static for each mode of use and should be held stable whilst the rst signal is high, when it will be latched into the core.

power_cic_gain_shift:

This control signal bus is used to set the data shift at the inputs to the Video Bandwidth CIC filter.

The appropriate values for each mode of operation are defined in the 'Control Signal Information' section below.

This control signal bus is static for each mode of use and should be held stable whilst the rst signal is high, when it will be latched into the core.

rbw_cic_decimation:

This control signal bus is used to set the data decimation rate at the outputs of the Resolution Bandwidth CIC filter.

The appropriate values for each mode of operation are defined in the 'Control Signal Information' section below.

This control signal bus is static for each mode of use and should be held stable whilst the rst signal is high, when it will be latched into the core.

vbw_output_decimation:

This control signal bus is used to set the data decimation rate at the outputs of the Video Bandwidth CIC filter.

The appropriate values for each mode of operation are defined in the 'Control Signal Information' section below.

This control signal bus is static for each mode of use and should be held stable whilst the rst signal is high, when it will be latched into the core.

dsp_clk:

This is the clock used to write the coefficients into the RBW FIR Filter. This does not have to be 64.2MHz, as it is connected to an input port of a dual port RAM, but would ideally be a derivative of 64.2 MHz (x2, x4… or /2, /4…).

coef_we:

This active high control signal is used to validate the RBW FIR Filter coefficient data to be written into the RBW FIR Filter.

This control signal should synchronous to the dsp clock and be high for at least one dsp clock period whilst valid data is present on the coef_data input ports.

coef_addr:

This control signal bus is used to point to 1 of 32 address locations in the dual port ram whilst writing the RBW FIR Filter coefficients.

This control signal should be synchronous to the dsp clock and be valid whilst valid data is present on the coef_data input ports.

coef_data:

This control signal bus is used to write 1 of 32 RBW FIR Filter coefficient values to the dual port RAM.

The appropriate filter coefficient values for each mode of operation are defined in are defined in Table 8 and Appendix B – List of Pre-calculated filters.

This control data should synchronous to the dsp clock and be valid whilst the coef_we is high.

data_out:

This is the 32 floating point (IEEE-754) data output of the core, selected by the output_select input control signal.

sync_out:

This active high control signal is used to indicate valid I samples or power samples presented on the output of the core.

en_out:

This active high control signal is used to indicate valid samples (I,Q and Power) presented on the output of the core.

Component Control Sequence

For each change in mode of operation, the following control set up sequence should be followed:

- Load the control registers with appropriate values for selected mode.
- Write 32 RBW coefficients to the dual port ram interface.
- Pulse the reset signal, to latch in the control register values.

Low power mode

After the set up sequence described above the core will wait for a sync to begin processing.

All of the clock enables and control in the core start from the receipt of the sync. So if no sync is received, no control or data signals will toggle inside the core. Therefore placing the core in a low power mode.

Figure 7 - Functional Block Diagram of RFEL FPGA Core

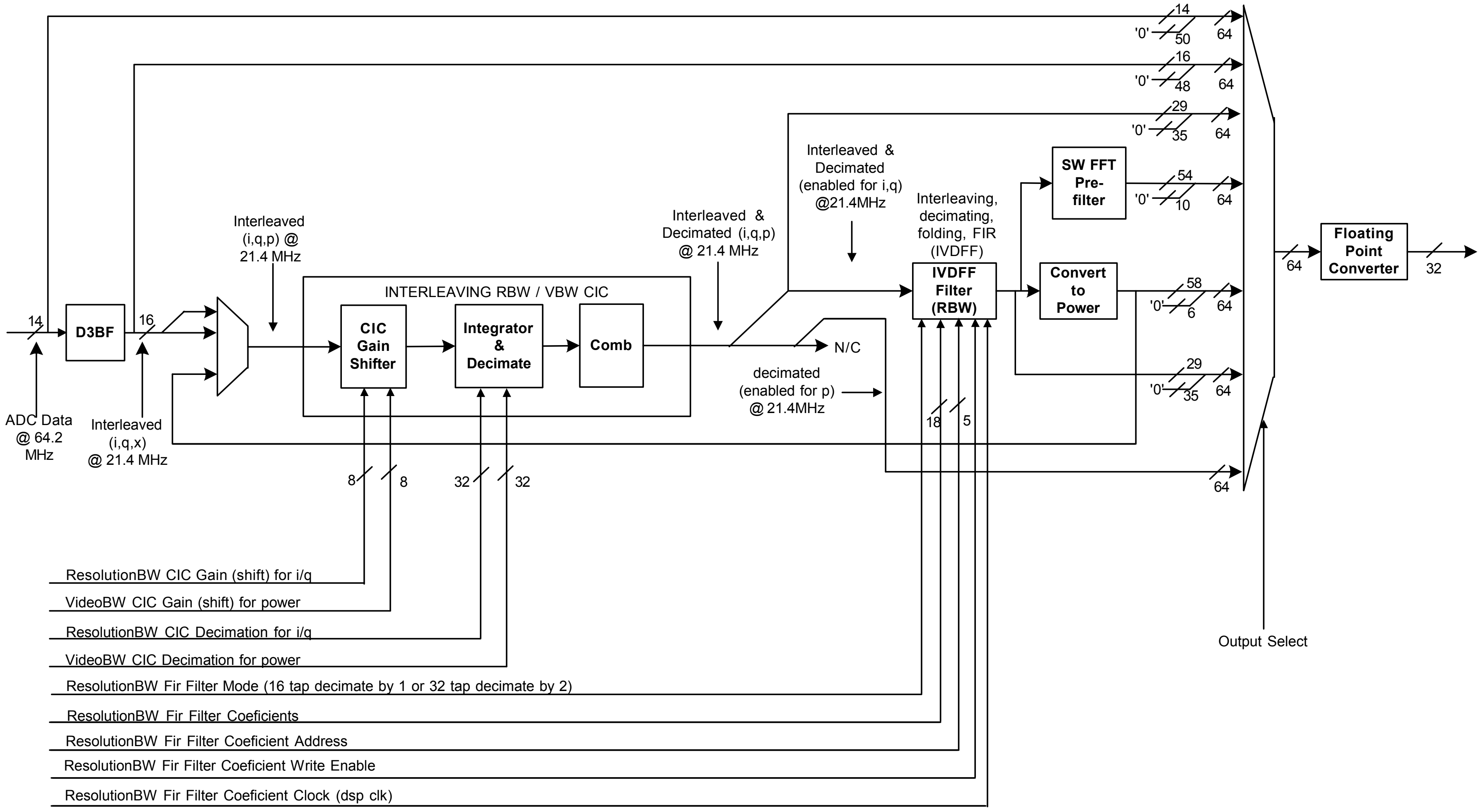
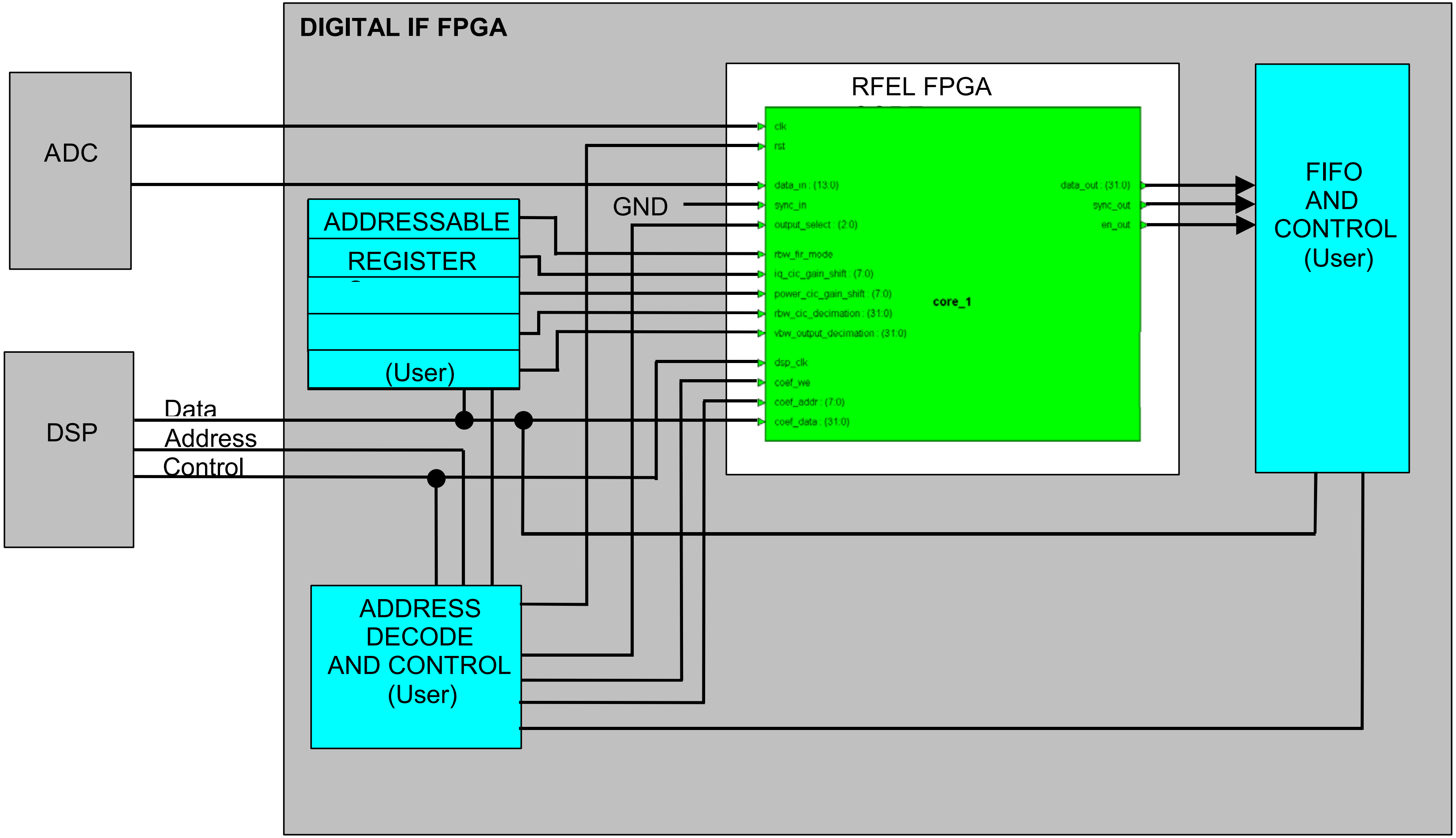


Figure 8 - Functional Block Diagram of RFEL FPGA Core Interface to User FPGA Code



TARGET TECHNOLOGY

The target technology for proving the design in RFELs hardware development system was a Xilinx Virtex-II FPGA (xc2v1000-4fg456).

The core has also been ported to a Xilinx Spartan-3 FPGA (xc3s1000-4fg676).

Place and Route Report

Area

The following is a section from the .mrp report generated by the Xilinx place and route tool, detailing the resource usage.

```
Release 6.2.01i Map G.29
Xilinx Mapping Report File for Design 'core_1'

Design Information
------------------
Command Line   : map -pr b -p xc3s1000-4fg676 core_1.ngd -o core_1_map.ncd
core_1.pcf
Target Device  : x3s1000
Target Package : fg676
Target Speed   : -4
Stepping Level : 1
Mapper Version : spartan3 -- $Revision: 1.16.8.1 $
Mapped Date    : Tue Mar 16 11:00:10 2004

Design Summary
--------------
Number of errors:      0
Number of warnings:  120
Logic Utilization:
  Number of Slice Flip Flops:       7,742 out of  15,360   50%
  Number of 4 input LUTs:           6,099 out of  15,360   39%
Logic Distribution:
  Number of occupied Slices:                       5,834 out of   7,680   75%
    Number of Slices containing only related logic:   5,834 out of   5,834  100%
    Number of Slices containing unrelated logic:          0 out of   5,834    0%
      *See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs:          9,125 out of  15,360   59%
  Number used as logic:              6,099
  Number used as a route-thru:         474
  Number used as 16x1 RAMs:            580
  Number used as Shift registers:    1,972
  Number of bonded IOBs:              205 out of     391   52%
    IOB Flip Flops:                   197
  Number of Block RAMs:                 1 out of      24    4%
  Number of MULT18X18s:                22 out of      24   91%
  Number of GCLKs:                      2 out of       8   25%

Total equivalent gate count for design:  479,633
```

```
Additional JTAG gate count for IOBs:  9,840
Peak Memory Usage:  205 MB

NOTES:

   Related logic is defined as being logic that shares connectivity -
   e.g. two LUTs are "related" if they share common inputs.
   When assembling slices, Map gives priority to combine logic that
   is related.  Doing so results in the best timing performance.

   Unrelated logic shares no connectivity.  Map will only begin
   packing unrelated logic into a slice once 99% of the slices are
   occupied through related logic packing.

   Note that once logic distribution reaches the 99% level through
   related logic packing, this does not mean the device is completely
   utilized.  Unrelated logic packing will then begin, continuing until
   all usable LUTs and FFs are occupied.  Depending on your timing
   budget, increased levels of unrelated logic packing may adversely
   affect the overall timing performance of your design.
```

Resource Observations

When using the RFEL core in the final FPGA design, the following advice relating to the customers own design would be appropriate:

- RFEL would encourage the user to partition its Block RAM memory into blocks of widths <18-bits, as using widths > 18-bits use shared routing with the multipliers and could therefore restrict the optimal use of these resources.

Timing

The following is a section from the .twr report generated by the Xilinx place and route tool, detailing the core timing analysis.

```
Timing summary:
---------------

Timing errors: 0  Score: 0

Constraints cover 383494 paths, 0 nets, and 37335 connections

Design statistics:
   Minimum period:  13.575ns (Maximum frequency:  73.665MHz)


Analysis completed Tue Mar 16 11:09:39 2004
--------------------------------------------------------------------------------
```

Power

The following is a section from the .pwr report generated by the Xilinx XPower tool, detailing the power analysis the core.

```
----------------------------------------------------------------
Release 6.2.01i - XPower SoftwareVersion:G.29
```

```
Copyright (c) 1995-2004 Xilinx, Inc.  All rights reserved.
Design:       core_1
Preferences:  ..\vhdl_synth\place_and_route\core_1.pcf
VCD File:     ..\vhdl_test\sim_gate\core_1.vcd
Part:         3s1000fg676-4
Data version: ADVANCED,v1.0,11-03-03

Power summary:                        I(mA)    P(mW)
----------------------------------------------------------------
Total estimated power consumption:               492
                               ---
                      Vccint 1.20V:      298      357
                      Vccaux 2.50V:       50      125
                      Vcco25 2.50V:        4       10
                               ---
                           Clocks:       20       24
                           Inputs:        1        2
                            Logic:       57       68
                          Outputs:
                             Vcco25       4       10
                          Signals:       70       84
                               ---
           Quiescent Vccint  1.20V:      150      180
           Quiescent Vccaux  2.50V:       50      125

Thermal summary:
----------------------------------------------------------------
   Estimated junction temperature:                25C
                  Ambient temp:  25C
                     Case temp:  25C
                     Theta J-A:   0C/W

Decoupling Network Summary:      Cap Range (uF)      #
----------------------------------------------------------------
Capacitor Recommendations:
Total for      Vccint :                             20
                                470.0  - 1000.0 :    1
                                 4.70  -  10.00 :    1
                                0.470  -  2.200 :    2
                               0.0470  - 0.2200 :    4
                               0.0100  - 0.0470 :    6
                               0.0010  - 0.0047 :    6
                                      ---
Total for      Vccaux :                             16
                                470.0  - 1000.0 :    1
                                0.470  -  2.200 :    1
                               0.0470  - 0.2200 :    3
                               0.0100  - 0.0470 :    5
                               0.0010  - 0.0047 :    6
                                      ---
Total for      Vcco25 :                             33
                                470.0  - 1000.0 :    1
                                 4.70  -  10.00 :    1
                                0.470  -  2.200 :    3
                               0.0470  - 0.2200 :    6
                               0.0100  - 0.0470 :   10
                               0.0010  - 0.0047 :   12

Analysis completed: Wed Mar 17 09:14:04 2004
```

CONTROL SIGNAL INFORMATION

CIC filter operation

To fully appreciate how a Cascaded-Integrator Comb (CIC) filter operates, the reader is invited to read “An economical class of digital filters for decimation and interpolation”, by Eugene B. Hogenauer, IEEE Transactions on acoustics, speech and signal processing, vol. Assp-29, no. 2, April 1981.

RFEL implementation has a fixed register size of 116 bits across the filter, with the final output being truncated down to a more manageable number of bits (see Paragraph 'System gains‘ below). Video Band-Width (VBW) filtering is also provided as on optional output mode. This has been implemented as part of the recycling architecture of the CIC, as it was an efficient use of hardware resources. The VBW CIC is identical to the RBW CIC with the exception that the differential delay in the comb section, M, is 3 rather than 1.

Figure 9 below shows the structure of the CIC filter used. The register size has been fixed to 116 bits as this provides adequate room for input maximum bit-growth within the filter itself.

As the registers size depends on the decimation used, decimation requiring smaller bit-widths is dealt with by bit-shifting the input so that the theoretical[1] MSB (most significant bit) of the filter output corresponds to the MSB of the CIC first register. This is shown in Figure 10 below.

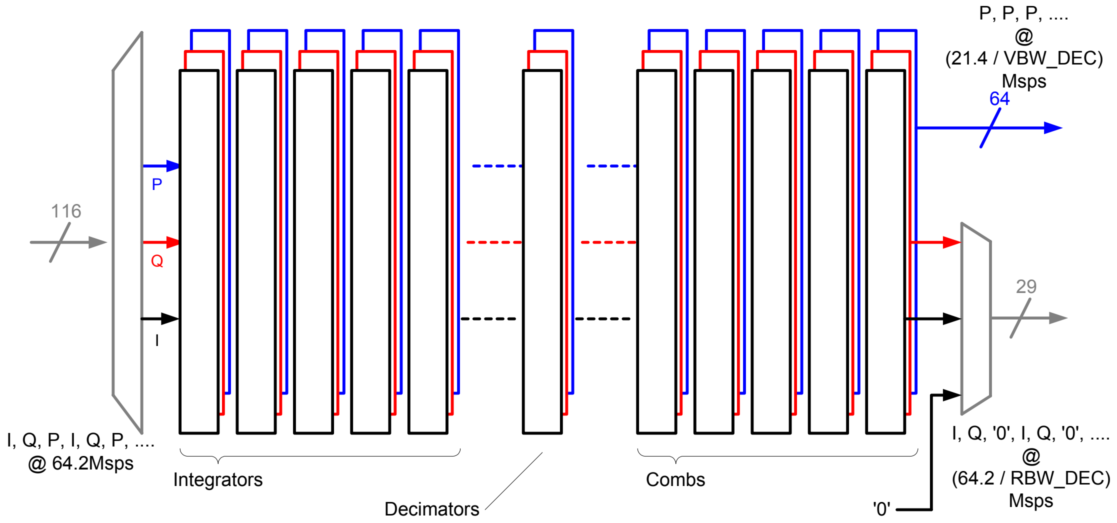


Figure 9: RFEL’s CIC architecture

---

[1] I.e. the MSB necessary to include the gain of the CIC itself.

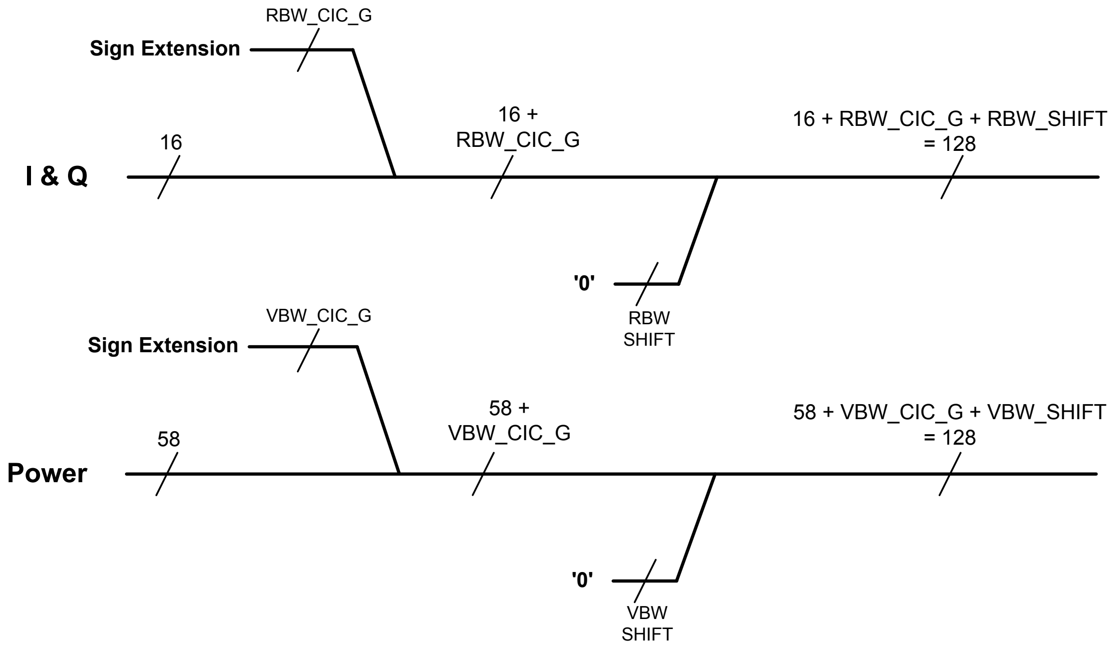


Figure 10: Functional diagram of bit shifter

For the above reasons, in RFEL's implementation of a digital IF replacement, the CIC filters need to be provided with an input bit shift value as well as the required decimation rate.

FIR filter operation

The resolution band-width FIR filters can operate as either an interleaved (I & Q) 16-tap non-decimating filter or as an interleaved 32-tap decimate-by-2 filter.

It should be noted here that for 16-tap mode of operation, it is not necessary to over-write the second block of 16 register values as these will not be used anyway.

When generating new filter coefficients for calibration purposes, the following rules must be satisfied:

- As only 18 bits signed integer are available for storing coefficient values, the values themselves should be in the range (-2^{17}) to (2^{17}-1).
- The filter gain G_{rbw_fir} should be ≤ 2^{19}; the correction factor to employ when adjusting the whole system gain is $\frac{G_{rbw\_fir}}{2^{19}}$. (See appendix A for a description of how to normalise filter coefficients so that the filter's dc gain is a predetermined value.)

Calculation of core parameters

Table 8 below shows which decimation factors to use in the CIC for each Resolution Band-Width (RBW).

RBW (Hz)	CIC Decimation	FIR Length	FIR Decimation	FIR design used[2]
3e6	1	16	1	1
1e6	3	16	1	2
3e5	5	32	2	3
1e5	15	32	2	4
3e4	50	32	2	4
1e4	150	32	2	4
3e3	500	32	2	4
1e3	1500	32	2	5
3e2	5000	32	2	6
1e2	15000	32	2	6
3e1	50000	32	2	6
1e1	150000	32	2	6

Table 8: CIC decimation and other values for RBW selection

The mode for the FIR filter is also shown, together with the coefficient set used in our models.

Table 9 below shows the decimation values to be used for the permitted RBW / VBW combinations.

---

[2] For a list of the set of pre-calculated filters, see Appendix B

RBW	VBW						
	1e6	1e5	1e4	1e3	1e2	1e1	1e0
3e6	**3**	**30**	**300**	**3000**	N/A	N/A	N/A
1e6	**1**	**10**	**100**	**1000**	N/A	N/A	N/A
3e5	N/A	**3**	**30**	**300**	**3000**	N/A	N/A
1e5	N/A	**1**	**10**	**100**	**1000**	N/A	N/A
3e4	N/A	N/A	**3**	**30**	**300**	**3000**	N/A
1e4	N/A	N/A	**1**	**10**	**100**	**1000**	N/A
3e3	N/A	N/A	N/A	**3**	**30**	**300**	**3000**
1e3	N/A	N/A	N/A	**1**	**10**	**100**	**1000**
3e2	N/A	N/A	N/A	N/A	**3**	**30**	**300**
1e2	N/A	N/A	N/A	N/A	**1**	**10**	**100**
3e1	N/A	N/A	N/A	N/A	N/A	**3**	**30**
1e1	N/A	N/A	N/A	N/A	N/A	**1**	**10**

Table 9: CIC decimation for VBW filtering

Once the decimation values are known for both RBW and VBW CICs, it is possible to calculate the bit shift values to input to the core.

These are:

$$\mathbf{RBW\_CIC\_SHIFT = CIC\_REG\_WIDTH - 16 - \{ceiling[\ 5{*}log_2(RBW_{decimation})\ ]\ \}} \qquad (1)$$

and,

$$\mathbf{VBW\_CIC\_SHIFT = CIC\_REG\_WIDTH - 58 - \{ceiling[\ 5{*}log_2(3{*}VBW_{decimation})\ ]\ \}} \qquad (2)$$

The reason for not listing the bit shifts in the above tables is that although the value of CIC_REG_WIDTH is currently 116, this could change with future requirements.

Note: When the VBW filtered power output is not desired, the VBW_CIC decimation should be set to 1 and the VBW shift to 0.

System gains

All outputs out of the floating-point converter are relative measurements, relative to the full scale input of the ADC.

The following equations provide the means for determining the numerical gain through the system, from the ADC to the final outputs.

$$\mathbf{G_{DIF\_IQ} = G_{into\_ADC} \times 2^{13} \times 1.5 \times G_{RBW\_CIC} \times G_{RBW\_CIC\_truncation} \times G_{RBW\_FIR} \times 2^{35}} \qquad (3)$$

where,

G_{DIF_IQ} is the gain of the I & Q streams from which power is obtained;

G_{into_ADC} is the gain as seen by the ADC input;

G_{RBW_CIC} is the gain of the RBW CIC, equal to

$$(RBW\_decimation)^5;$$

$G_{RBW\_CIC\_trunctaion}$ is the gain due to CIC output truncation, equal to

$$2^{29-ceil(5\cdot\log_2(RBW\_decimation))};$$

G_{RBW_FIR} is the gain of the quantised RBW FIR filters, equal to

$$\frac{\sum Coefficients}{2^{19}}.$$

$$\mathbf{G_{FFT\_IQ} = G_{into\_ADC} \times 2^{13} \times 1.5 \times G_{RBW\_CIC} \times G_{RBW\_CIC\_truncation} \times G_{FFT\_FIR} \times 2^{10}} \qquad (4)$$

where,

G_{FFT_IQ} is the gain of the I & Q streams used for calculating the narrow-band FFT in the DSP;

G_{FFT_FIR} is the gain of the 127-taps decimate-by-4 FIR filters, equal to $\sum Coefficients$.

$$\mathbf{G_{power} = (G_{DIF\_IQ})^2 \times 2^6} \qquad (5)$$

where,

G_{power} is the gain of the unfiltered power.

$$\mathbf{G_{power\_VBW} = G_{power} \times G_{VBW\_CIC} \times G_{VBW\_CIC\_truncation}} \qquad (6)$$

where,

G_{power_VBW} is the gain of the power after VBW filtering;

G_{VBW_CIC} is the gain of the VBW CIC, equal to $(3\cdot VBW\_decimation)^5$;

$G_{VBW\_CIC\_trunctaion}$ is the gain due to CIC output truncation, equal to

$$2^{64-ceil(5\cdot\log_2(3\cdot VBW\_decimation))};$$

Throughout testing, G_{into_ADC} has been assumed to be 1, as inputs into the ADC have been normalised to unity peaks (i.e. signals ranging from –1 to +1 Volts).

This may vary depending on the particular circumstances. As an example, for a 4.8dBm input power into a 50 Ohm load, the peak input voltage is 0.549541V, thus

G_{into_ADC} = 0.549541

The merit of calculating the above gains is that by means of normalising the core output by these values, one obtains the various measurements directly scaled to the correct units (Watts or Volts).

Narrow Band FFT output mode

Note

- In this mode the RBW CIC decimation should be set to 143, while all other parameters can be arbitrarily set as they have no effects on the processing of the I and Q for the narrow–band FFT.

Verification of the core was achieved in several distinct phases in the design cycle.

Initially, a bit-true Matlab model of the core is used to provide reference output data, using a specific set of input stimuli. These models exactly match the behaviour of the hardware architecture and their outputs are bit-true representations of the actual core.

The input stimuli are used to functionally (pre-synthesis) test the VHDL code using the ModelSim simulator. The results of these simulations are compared with the reference data generated by the bit-true Matlab model and pass/fail indications are reported.

After the VHDL has been synthesised and place-and-route of the core is complete, timing simulations, based on the chip vendor's simulation netlist and gate delay files for the core are performed. These also take the form of the functional tests, but being based on the compiled netlist and timing files from the FPGA vendor, they verify the expected timings of the delivered core.

TOOLS

The following tools and versions were used to generate this delivery.

Modelsim PE	Version: 5.7f
Leonardo Spectrum Level 2	Version: LS2003b_65
Xilinx ISE	Release Version: 6.2.01i
	Application Version: build i+G-29+61500
Matlab	Version: 6.5.0.180913a r13

DELIVERED FILE DIRECTORY STRUCTURE

The delivered file structure is shown in Figure 11.

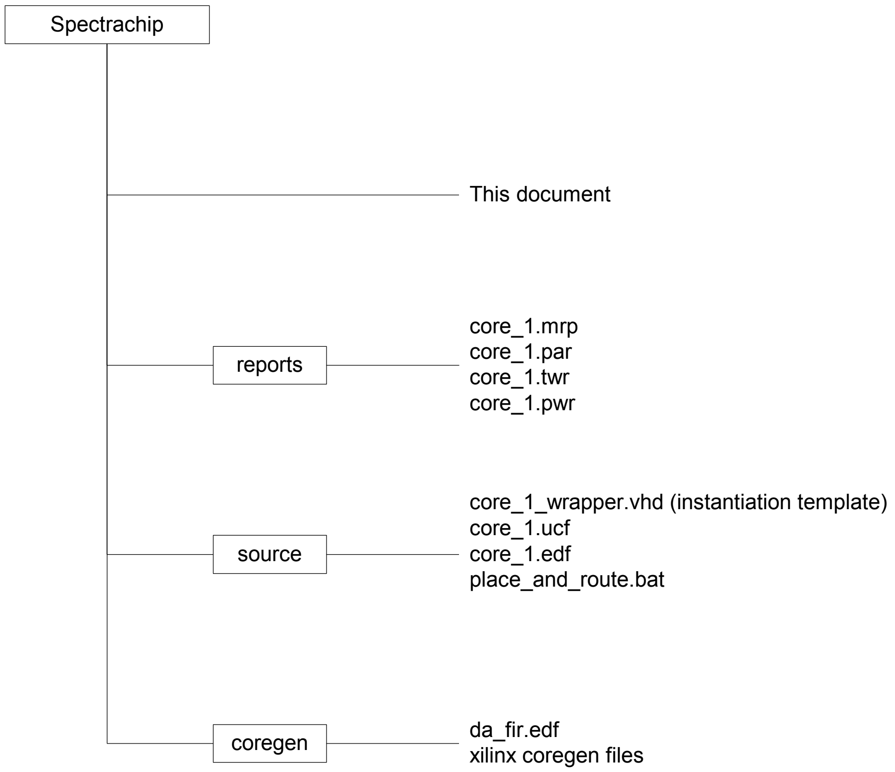


Figure 11: Delivered file structure

USING THE CORE

The following steps should be followed to ensure the EDIF netlist is included in the final design:

- Include the instance(s) of the core within the target design (using *Spectrachip/source/core_1_wrapper.vhd'* as a reference).
- Place the core EDIF file *'Spectrachip/source/core_1.edf'* in the same directory as the final design EDIF, or add the macro search path in the process properties dialog box (right mouse click over implement design > properties) in XilinxISE.
- Point to the xilinx coregen directory where the da_fir EDIF file is stored *'Spectrachip/coregen/da_fir.edf'* in the place and route script (an example is shown in the place and route script *'Spectrachip/source/place_and_route.bat)*, or add the macro search path in the process properties dialog box (right mouse click over implement design > properties) in XilinxISE.
- Use the parameters contained in the constraints file *'Spectrachip/source/core_1.ucf'* as a reference.
- Continue through normal place and route using the XilinxISE tools and the core will be automatically integrated into the design.

APPENDIX A – FILTER TAPS QUANTISATION

Most filter design packages would generate FIR filter coefficients (un-quantised) with a dc gain of unity (e.g. SystemView, Matlab, QED2000, etc).

To verify this is actually the case, suffice to take the sum of all coefficients, which provides the dc gain of a FIR filter:

$$G_{FIR\_dc} = \sum Coefficients\,.$$

By quantising the coefficients to 18 bits, i.e.

Quantised_coefficients = round[Coefficients * $(2^{17}-1)$],

The dc gain becomes roughly $(2^{17}-1)$, yet the bit-widths of the taps are not used optimally. In order to improve on this situation, the un-quantised filters coefficients should be first scaled by an integer number such that the largest coefficient magnitude is as close as possible to unity.

If, after this process, the dc gain exceeds the predefined maximum of 2^{19} by a small margin, then the un-quantised coefficient shall be scaled down in small steps (e.g. measured_gain/2^{19}) and re-quantised until the dc gain is $\leq 2^{19}$.

As an example, consider the following filter taps (the coefficient values of filter 1 in Appendix B are actually derived from this filter):

Taps = { 0.000081, 0.000573, 0.003068, 0.012425, 0.038037, 0.088034, 0.154033, 0.203749, 0.203749, 0.154033, 0.088034, 0.038037, 0.012425, 0.003068, 0.000573, 0.000081}

Before quantising to 18 bits, the coefficients are scaled by the largest integer value such that the greatest taps magnitude is ≤1, i.e.

floor(1/0.203749) = 4.

Thus,

Quantised_Taps = round[4*Taps*(2^{17}-1)] =

{42, 300, 16086514, 19942, 46154, 80757, 106822, 106822, 80757, 46154, 19942, 6514, 1608, 300, 42 }

The dc gain is:

$\sum Quantised\_Taps$ = 524278 ≤ 524288(=2^{19}),

so there is no need to rescale the un-quantised coefficients to reduce the gain.

APPENDIX B – LIST OF PRE-CALCULATED FILTERS

NOTE: *These filters include compensation for the analog pre-filters and the CICs*.

Filter 1

Taps = [42, 300, 16086514, 19942, 46154, 80757, 106822, 106822, 80757, 46154, 19942, 6514, 1608, 300, 42]

Gain = 524278

Filter 2

Taps = [18, 165, 10655031, 17410, 44177, 82182, 112090, 112090, 82182, 44177, 17410, 5031, 1065, 165, 18]

Gain = 524276

Filter 3

Taps = [1, 7, 23, 72, 205, 530, 1255, 2727, 5435, 9939, 16671, 25655, 36218, 46908, 55735, 60753, 60753, 55735, 46908, 36218, 25655, 166719939, 5435, 2727, 1255, 530, 205, 72, 23, 7, 1]

Gain = 524268

Filter 4

Taps = [2, 7, 24, 74, 210, 539, 1273, 2758, 5480, 9995, 16729, 25696, 36222, 46861, 55638, 60625, 60625, 55638, 46861, 36222, 25696, 167299995, 5480, 2758, 1273, 539, 210, 74, 24, 7, 2]

Gain = 524266

Filter 5

Taps = [5, 18, 52, 143361, 840, 1811, 3615, 6684, 11442, 18141, 26634, 36213, 45597, 53167, 57412, 57412, 53167, 45597, 36213, 26634, 18141, 11442, 6684, 3615, 1811, 840, 361, 143, 52, 18, 5]

Gain = 524270

Filter 6

Taps = [12, 35, 94, 234, 542, 1171, 2357, 4422, 7738, 12625, 19207, 27247, 36041, 44454, 51127, 54830, 54830, 51127, 44454, 36041, 27247, 19207, 12625, 7738, 4422, 2357, 1171, 542, 234, 94, 35, 12]

Gain = 524272